Journal for Educators, Teachers and Trainers
The PROFESIOLab electronic, peer-reviewed, open-access Magazine

ISSN 1989-9572

DOI: 10.47750/jett.2022.13.05.054

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Journal for Educators, Teachers and Trainers, Vol.13 (5)

https://jett.labosfor.com/

Date of Reception: 12 July 2022

Date of Revision: 13 Aug 2022

Date of Acceptance: 20 September 2022

***Nagaraju Budidha, Prakash Chary Karnakanti, Rajesh Thota, Danam Akshith, Pureti Meghana* (2022). DESIGNING EFFICIENT STEP-UP MULTILEVEL INVERTERS WITH NOVEL SWITCHED CAPACITOR CONVERTERS AND FEWER COMPONENTS. Journal for Educators, Teachers and Trainers, Vol.13(5). 581-591.**

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DESIGNING EFFICIENT STEP-UP MULTILEVEL INVERTERS WITH NOVEL SWITCHED CAPACITOR CONVERTERS AND FEWER COMPONENTS

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ABSTRACT—This paper presents a novel design of switched capacitor converters aimed at achieving component reduction for step-up multilevel inverter topologies. Traditional multilevel inverters often require numerous components, leading to increased complexity, size, and cost. By implementing innovative switched capacitor techniques, this study introduces a more efficient approach that minimizes component count while maintaining high performance and reliability. The proposed topology enables effective voltage boosting with reduced losses and enhanced power quality, making it suitable for various applications in renewable energy systems and electric vehicles. Simulation results demonstrate significant improvements in efficiency and overall system performance compared to conventional inverter designs. This research contributes to the ongoing development of advanced power electronics, emphasizing the potential for simpler, more compact, and cost-effective solutions in multilevel inverter technology. The findings provide a solid foundation for future work aimed at optimizing switched capacitor converter designs for broader industrial applications.
Index Terms— Boosting factor, multilevel inverter, switched capacitor, reduced devices, voltage balance

I.INTRODUCTION

The increasing demand for efficient power conversion technologies has propelled the development of advanced inverter systems, particularly in renewable energy applications and electric vehicle drives. Multilevel inverters have emerged as a promising solution due to their ability to produce high-quality output voltage waveforms, reduce harmonic distortion, and improve overall system performance. However, traditional multilevel inverter designs often involve a significant number of components, which can lead to increased complexity, cost, and size. This presents a critical challenge in designing compact and efficient inverter systems that can meet modern energy demands.

To address these challenges, researchers have been exploring innovative topologies that leverage switched capacitor techniques. Switched capacitor converters utilize capacitors as energy storage elements, allowing for efficient voltage conversion without the need for inductive components. This approach not only simplifies the circuit design but also significantly reduces the number of components required, thereby enhancing system reliability and minimizing physical footprint.

This paper proposes a novel switched capacitor converter design that integrates seamlessly into step-up multilevel inverter topologies. The objective is to develop a more efficient inverter system that maintains high performance while reducing the complexity associated with traditional designs. By minimizing component count, the proposed topology aims to lower manufacturing costs and facilitate easier integration into various applications, such as solar inverters and battery management systems.

Through detailed analysis and simulation, this study explores the performance of the proposed switched capacitor converters in step-up multilevel inverter configurations. The findings are expected to demonstrate improvements in efficiency, power quality, and overall system reliability compared to conventional multilevel inverter designs. Ultimately, this research contributes to the ongoing evolution of power electronics, providing a pathway toward more efficient, compact, and cost-effective solutions in the field of renewable energy and beyond.

II. BASIC CELL OF PROPOSED SCC

Basic Cell (BC) of the proposed SCC is depicted in Fig. 1(a). It comprises of 4 switches (S_1, S_2, S_{1c} and S_{2c}), 1 diode (D), 2 capacitors (C_1 and C_2) and 1 dc power supply (V_{in}). Switches S_2, S_{1c} and S_{2c} do not have anti-parallel diode whereas switch S_1 has anti-parallel diode. Capacitors C_1 and C_2 can be charged up-to V_{in} by connecting them in parallel with Vin individually by applying appropriate switching states. With these capacitor voltages, BC can produce 3 positive voltage levels ($+V_{in}$, $+2V_{in}$ and $+3_{Vin}$) across output terminals A and B. Table I shows state of the switches and capacitors corresponding to different output voltage levels. Where '1' and '0' stand for on and off states of switches respectively. Further, charging state, discharging state and not-connected state of the capacitors are indicated by 'C', 'D' and 'NC' respectively.

Fig. 1(b) shows equivalent circuit and current flow paths when S_{2c} is on. During this switching state,C_2 is connected in parallel with Vin through D. Hence, C_2 accumulates energy from V_{in} and is charged near about Vin. Charging current for C_2 is iC_2 as shown in Fig. 1(b). Whereas C_1 remains in NC state.

Further, during this switching state, output voltage of BC (i.e. V_{AB}) is equal to V_{in}.

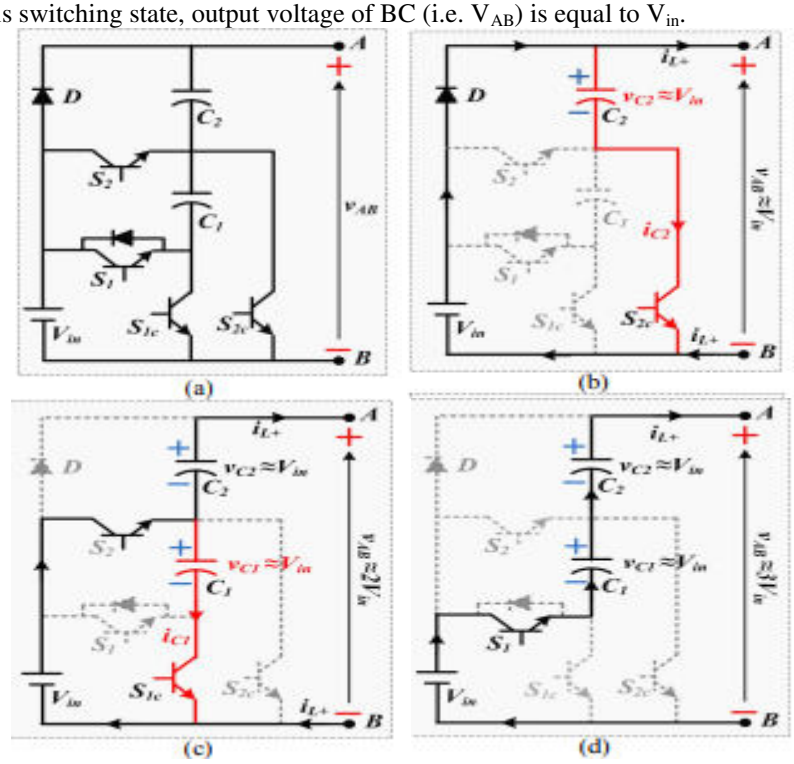


Fig.1. Figure presents (a) BC of proposed SCC; Equivalent circuit and current flow paths of proposed BC when $v_{AB}$is (b) $+V_{in}$, (c) $+2V_{in}$ and (d) $+3V_{in}$

Fig. 1(c) depicts equivalent circuit and current flow paths when S_2 and S_{1c} are turned on. With this switching state, C_1 is connected in parallel with V_{in} whereas C_2 is connected in series with Vin. Hence, C_1 accumulates energy from V_{in} whereas C_2 transfers its stored energy towards the load. During this switching state, V_{AB} is equal to summation of $V_{in}$and voltage across C_2 i.e. V_{AB} is nearly equal to $2V_{in}$. The charging current for C_1 is iC_1 as depicted in Fig. 1(c).

When S_1 is turned on, both C_1 and C_2 are connected in series with V_{in}. Hence, output voltage of BC is equal to near about $3V_{in}$. In this state, both capacitors are in discharging state and transfer their stored energy towards the load as depicted in Fig. 1(d) and Table I.

TABLE 1 SWITCH AND CAPACITOR STATES FOR BASIC CELL

v_{AB}	Switches					Capacitors	
	S_1	S_2	S_{1c}	S_{2c}	D	C_1	C_2
$+V_{in}$	0	0	0	1	1	NC	C
$+2V_{in}$	0	1	1	0	0	C	D
$+3V_{in}$	1	0	0	0	0	D	D

From this above discussion, it can be concluded that
(a) The proposed BC has self- boosting ability ; boosting factor i.e. the ratio of peak output of BC and input dc source, is equal to 3,
(b) The capacitors can be connected in series/parallel with input supply using simple switching strategy and at the same time output voltage level can be produced,
(c) By turning on only one switch (S_1), the highest output voltage level (i.e. $+3V_{in}$) can be produced. (d) Stress voltages for S_1, S_2, S_{1c} and S_{2c} are $2V_{in}$, V_{in}, V_{in} and $2V_{in}$ respectively. Hence, TSV of the BC is 6Vin. Further, peak inverse voltage (PIV) of the diode D is 2Vin.

III.PULSE-WIDTH MODULATION (PWM)

Pulse-width modulation (**PWM**), or **pulse-duration modulation** (**PDM**), is a modulation technique used to encode a message into a pulsing signal. Although this modulation technique can be used to encode information for transmission, its main use is to allow the control of the power supplied to electrical devices, especially to inertial[*definition needed*] loads such as motors. In addition, PWM is one of the two principal algorithms used in photovoltaic solar battery chargers,[1] the other being maximum power point tracking.

The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast rate. The longer the switch is on compared to the off periods, the higher the total power supplied to the load.

The PWM switching frequency has to be much higher than what would affect the load (the device that uses the power), which is to say that the resultant waveform perceived by the load must be as smooth as possible. The rate (or frequency) at which the power supply must switch can vary greatly depending on load and application, for example Switching has to be done several times a minute in an electric stove; 120 Hz in a lamp dimmer; between a few kilohertz (kHz), to tens of kHz for a motor drive; and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies.

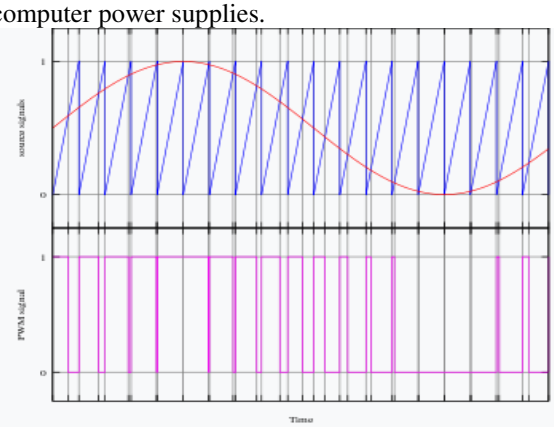


Fig.2: A simple method to generate the PWM pulse train corresponding to a given signal is the intersective PWM: the signal (here the red sine wave) is compared with a sawtooth waveform (blue). When the latter is less than the former, the PWM signal (magenta) is in high state (1). Otherwise it is in the low state (0).

IV.MULTI LEVEL INVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC) the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utilityhigh voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high power electronic oscillator. It is so named because early mechanical AC to DC converterswere made to work in reverse, and thus were "inverted", to convert DC to AC.

4.1Cascaded H-Bridges inverter

A single phase structure of an m-level cascaded inverter is illustrated in Figure 3. Each separate DC source (SDCS) is connected to a single phase full bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The AC outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate DC sources. An example phase voltage waveform for an 11 level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 4. The phase voltage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5} \ldots (4.1)$$

For a stepped waveform such as the one depicted in Figure 4.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\frac{\sin(n\omega t)}{n},\ where\ n = 1,3,5,7\ \ldots\ldots (4.2)$$

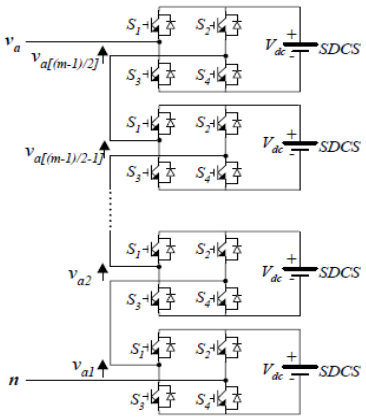


Fig3:Single-phase structure of a multilevel cascaded H-bridges inverter

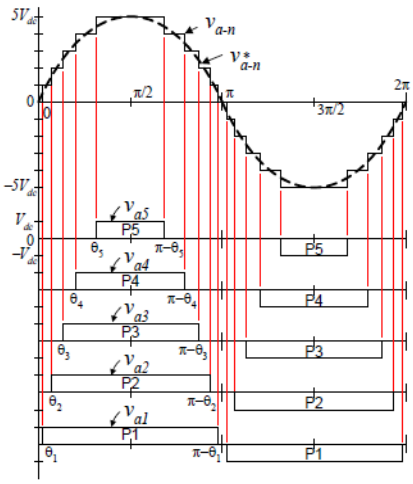


Fig.4. Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources.

V.PROJECT DISCRIPTION AND CONTROL DESIGN

5.1 GENERALIZED STRUCTURE OF PROPOSED SCC

This section presents the development of generalized structure of proposed SCC. The structure is developed by connecting n number of capacitors (C_1 to C_n) in series connection as shown in Fig. 2. A switch Sic (i =1 to n) is connected between negative terminal of C_i(i=1 to n) and negative terminal of V_{in}. Similarly, a switch S_i (i=2 to n) is connected between mid-point of 2 capacitors C_i and $C_{(i-1)}$ (i=2 to n) and positive terminal of Vin as shown in Fig. 2. Switch S_1 is connected in between positive terminal of V_{in} and negative terminal of C_1.

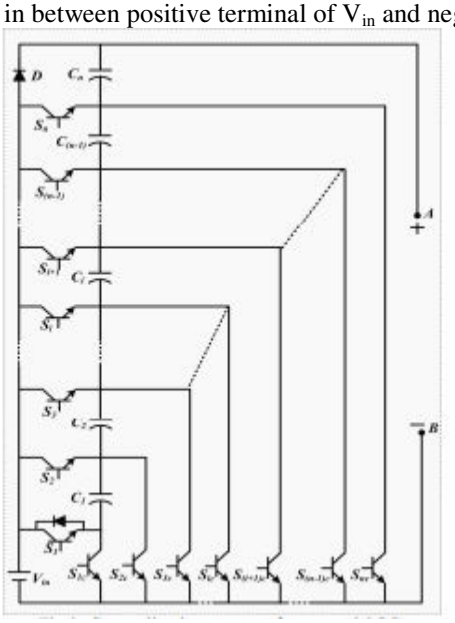
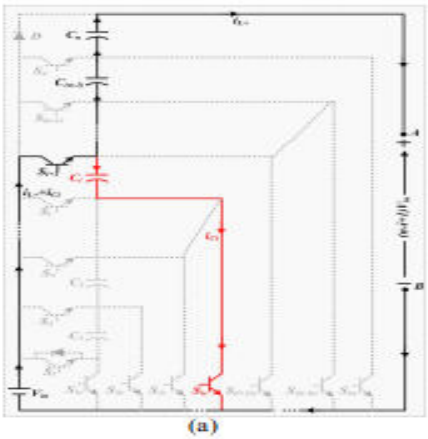
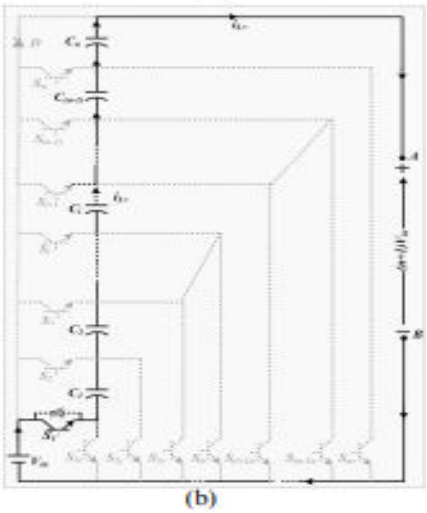


Fig.5. Generalized structure of proposed SCC



(a)



(b)

Fig.6. Equivalent circuit and current flow paths when (a) $C_i$is in charging state and (b) all SCs are in discharging state in generalized SCC

All the capacitors in this structure can be charged to V_{in} by turning on appropriate switches. For example, i th capacitor, C_i can be charged to V_{in} by turning on switches S_{i+1} and Sic as shown in Fig. 3(a). During this switching state, the generated output voltage appeared across A to B is $(n-i+1)V_{in}$. Capacitors connected above of C_i i.e. (C_n to C_{n-i}) are in discharging state whereas capacitors connected to lower of C_ii.e. (C_1 to C_{i-1}) are in NC state. It is observed that the structure needs to conduct only 2 switches to charge any utilized capacitors. Hence, $N_{path_C}$for the SCC (i.e. $N_{path\_C\_scc}$) is 2 and it does not depend on n.

When S_1 is turned on and other switches are in off condition, all the capacitors are connected in series with Vin and highest voltage level of SCC i.e. $(n+1)V_{in}$is generated across A to B as shown in Fig. 3(b). During this switching state, all capacitors are in discharging state. As the structure needs to conduct only 1 switch to produce the highest voltage level, $N_{path}$for the SCC (i.e. N_{path_scc}) is 1 and it is independent of n.

The number of switches (N_{sw_scc}), drivers (N_{dr_scc}), capacitors (N_{cap_scc}) and TSV (TSV_SCC) of generalized SCC in terms of n can be expressed by (1)-(3). The structure requires only one power diode (i.e. N_{dio_scc}=1).

$$N_{sw\_scc} = N_{dr\_scc} = 2n \quad (1)$$

$$N_{cap\_scc} = n \quad (2)$$

$$TSV\_SCC = \frac{1}{4}(5n^2 + 2n + 1) \quad \forall\ n = \text{odd}$$
$$= \frac{1}{4}(5n^2 + 2n) \quad \forall\ n = \text{even} \quad (3)$$

COMPARISON OF PROPOSED SCC WITH OTHER SCCS

This section presents the comparison of proposed BC and generalized structure of SCC with the recently developed SCCs presented in [15-17, 20-21, 23, 24].

A.Comparison of proposed BC with others

Table II shows the comparison of proposed BC with other SCCs in respect of component requirement, boosting factor (B_{scc}) and (TSV+PIV). As per Table II, the proposed BC requires lower number of switches and drivers as compared to the SCCs presented in [15-16, 23-24]. The switch per level (N_{sw_scc}/N_{L_scc}) for proposed BC is 1.33 which is lower than the SCCs presented in [15-16, 23-24] as shown in Table II. The SCC presented in [17] requires same number of switches and drivers as that for proposed one. However it requires more number of power diodes. The proposed BC has higher B_{scc}than SCC presented in [23]. $B_{scc}$for [23] is 2 whereas that for proposed BC is 3. The is due to inability of the SCC presented in [23] to charge the capacitors up-to the full dc supply voltage.

The SCC presented in [20-21] requires lower number of switches as compared to the proposed BC. As per Table II, $N_{sw_scc}/N_{L_scc}$for [20-21] is 1.25 whereas that for proposed BC is 1.33. However, the SCC presented in [20-21] requires two capacitors of different voltage ratings. The maximum voltage rating of utilized capacitors (V_{Cmax_rating}) for [20-21] is $2V_{in}$ whereas the proposed BC utilizes two capacitors of equal voltage rating as shown in Table II. Each capacitor voltage rating of proposed BC is V_{in}. This can reduce the cost of the capacitors of proposed BC as compared to the SCC presented in [20-21].

The major advantage of proposed BC is that it requires lower N_{path_scc} than others. As per Table II, $N_{path_scc}$of proposed

TABLE II

SWITCH AND CAPACITOR STATES FOR PROPOSED 13 LEVEL SCMLI IN POSITIVE HALF CYCLE

$\frac{v_o}{V_{dc}}$	on switches during the first quarter cycle	C_{11}	C_{21}	C_{12}	C_{22}	on switches during the second quarter cycle	C_{11}	C_{21}	C_{12}	C_{22}
+6	$S_{11}, S_{11}, S_{12}, S_{12}, S_{13}$	D	D	D	D	$S_{11}, S_{11}, S_{12}, S_{12}, S_{13}$	D	D	D	D
+5	$S_{11}, S_{21}, S_{12}, S_{12}, S_{13}, S_{k1}$	C	D	D	D	$S_{11}, S_{11}, S_{12}, S_{22}, S_{13}, S_{k2}$	D	D	C	D
+4	$S_{11}, S_{21}, S_{12}, S_{12}, S_{13}$	NC	C	D	D	$S_{11}, S_{11}, S_{12}, S_{22}, S_{13}$	D	D	NC	C
+3	$S_{11}, S_{21}, S_{k1}, S_{12}, S_{22}, S_{13}$	C	D	NC	C	$S_{11}, S_{21}, S_{12}, S_{22}, S_{k2}, S_{13}$	NC	C	C	D
+2	$S_{11}, S_{21}, S_{12}, S_{22}, S_{13}$	NC	C	NC	C	$S_{11}, S_{21}, S_{12}, S_{22}, S_{13}$	NC	C	NC	C
+1	$S_{11}, S_{21}, S_{12}, S_{13}, S_{22}, S_{k2}$	NC	C	C	NC	$S_{21}, S_{22}, S_{23}, S_{13}, S_{21}, S_{k1}$	C	NC	NC	C
0	$S_{11}, S_{12}, S_{13}, S_{21}, S_{k1}, S_{22}, S_{k2}$	C	NC	C	NC	$S_{11}, S_{12}, S_{13}, S_{22}, S_{k2}, S_{21}, S_{k1}$	C	NC	C	NC

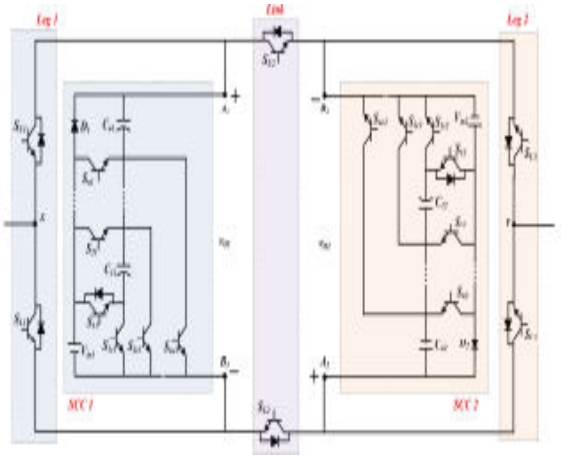


Fig.7. Proposed SCMLI with generalized SCCs

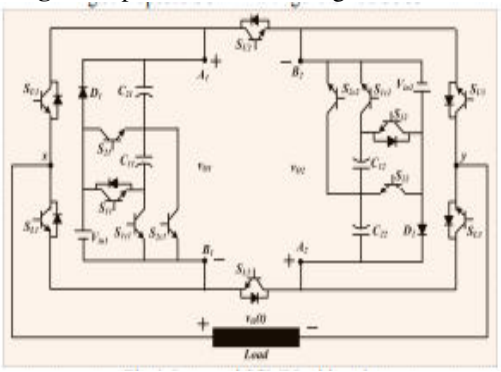


Fig.8. Proposed SCMLI with n=2

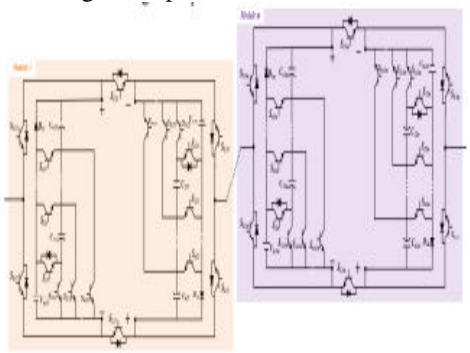


Fig.9. Cascaded extension of proposed SCMLI

load by turning on the complementary switches present in Leg 1, Leg 2 and Link circuits. Similarly, for n=2, the proposed structure can produce 31 output voltage levels with asymmetric dc sources (V_{in1}=$V_{dc}$and V_{in2}=4V_{dc}).

The cascaded extension of proposed SCMLI is shown in Fig. 7. It consists of m number of modules. The required switches (N_{sw}) and drivers (N_{dri}), capacitors (N_{cap}), diodes (N_{dio}), dc sources (N_{dc}), $N_{path}$and N_{path_C}can be expressed by (4) and (5).

$$N_{sw} = N_{dr} = (4n+6)m \;;\; N_{cap} = 2nm \qquad (4)$$

$$N_{dc} = N_{dio} = 2m \;;\; N_{path} = 5m \;;\; N_{path\_C} = 2 \qquad (5)$$

The cascaded SCMLI is analyzed for symmetric and asymmetric dc source configurations. In symmetric configuration, all modules have same magnitude of dc sources as presented by (6). The output voltage level and TSV of the structure can be presented by (7) and (8) respectively.

$$V_{inlk} = V_{in2k} = V_{dc} \quad \forall \; k = 1 \text{ to } m \qquad (6)$$

$$N_L = 4nm + 4m + 1 \qquad (7)$$

$$TSVpu_{symcas} = \frac{5n^2+18n+17}{4(n+1)} \;\; \forall \;\; n = \text{odd} \;;$$

$$\frac{5n^2+18n+16}{4(n+1)} \;\; \forall \;\; n = \text{even} \qquad (8)$$

Further, the proposed cascaded SCMLI is analyzed for asymmetric dc source configuration. In this configuration, magnitude of dc sources, generated output voltage levels and TSV of the proposed structure are presented by (9), (10) and (11) respectively.

VI.SIMULATION RESULTS

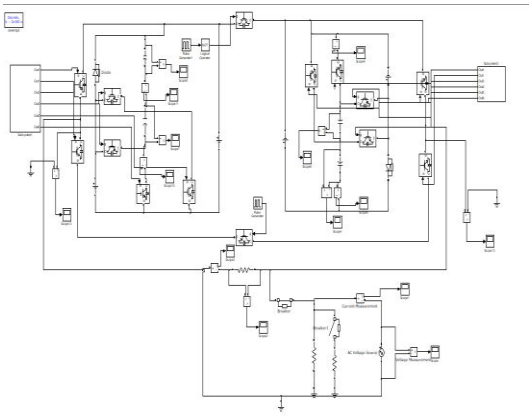


Fig10: Proposed Simulation Diagram

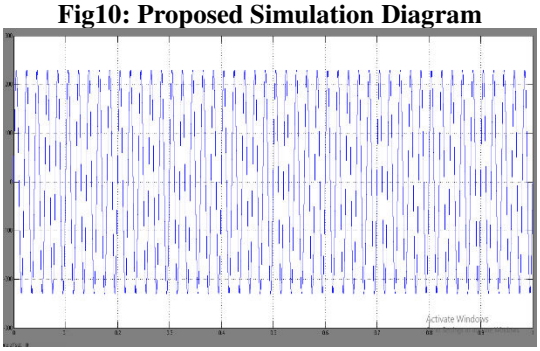


Fig11:Vg

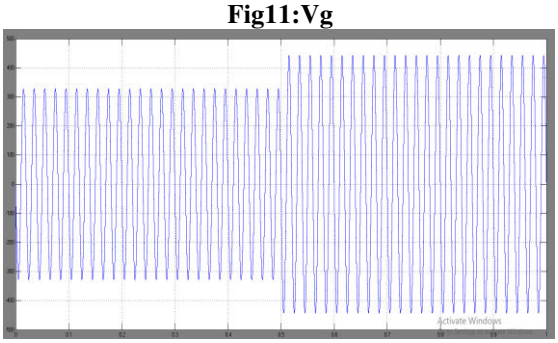
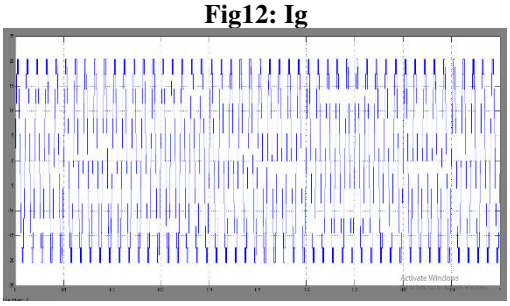


Fig12: Ig



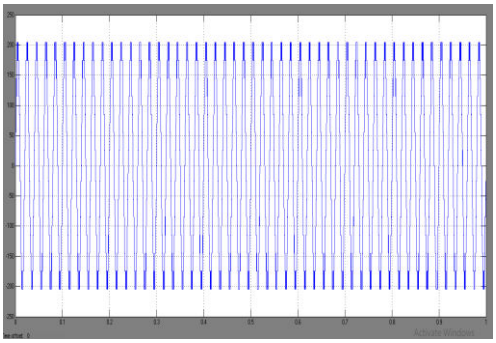


Fig: 13 level output voltage and output current

VII.CONCLUSION

In conclusion, this study successfully introduces a novel switched capacitor converter design that significantly reduces the component count in step-up multilevel inverter topologies while enhancing overall performance. The proposed approach addresses critical challenges associated with traditional multilevel inverters, such as complexity, size, and cost, by leveraging the advantages of switched capacitor techniques. Simulation results demonstrate marked improvements in efficiency, voltage quality, and reliability, showcasing the viability of the proposed design for a range of applications, including renewable energy systems and electric vehicles. By simplifying the inverter architecture and minimizing the reliance on passive components, this research contributes to the ongoing development of more compact and efficient power conversion solutions. Future work may focus on further optimization of the switched capacitor converter design and its integration into practical systems, paving the way for advancements in power electronics that support sustainable energy technologies and improved grid integration.

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