Journal for Educators, Teachers and Trainers
The PROFESIOLab electronic, peer-reviewed, open-access Magazine

ISSN 1989-9572
DOI:10.47750/jett.2021.12.01.029

VLSI Architecture for Turbo Decoder using MAP Algorithm for Enhanced Error Correction in Communication Systems

Dr. S. Sreenath Kashyap[1],

Dr. U. Rajender[2]

Journal for Educators, Teachers and Trainers, Vol.12(1)
https://jett.labosfor.com/

Date of reception: 10 Dec 2020
Date of revision: 1 Jan 2021
Date of acceptance: 29 Jan 2021

Dr. S. Sreenath Kashyap, Dr. U. Rajender (2021). VLSI Architecture for Turbo Decoder using MAP Algorithm for Enhanced Error Correction in Communication Systems. Journal for Educators, Teachers and Trainers, Vol.12(1). 240-246.

Journal for Educators, Teachers and Trainers, Vol. 12(1)

ISSN 1989 –9572

https://jett.labosfor.com/

VLSI Architecture for Turbo Decoder using MAP Algorithm for Enhanced Error Correction in Communication Systems

Dr. S. Sreenath Kashyap[1], Dr. U. Rajender[2]
[1]Associate Professor, Department of Electronics and Communication Engineering, Kommuri Pratap Reddy Institute of Technology, Hyderabad, Telangana. sreenathkashyaps@gmail.com
[2]Assistant Professor, Department of Electronics and Communication Engineering, Vaageswari College of Engineering, Karimnagar, Telangana. urajender10@gmail.com

ABSTRACT
Turbo codes are highly effective error correction codes, utilized in communication systems due to their superior error correction capabilities. This study introduces a Very Large-Scale Integration (VLSI) architecture aimed at enhancing error correction through the development of a Turbo decoder. The decoder integrates interleavers, deinterleavers, and soft-in-soft-out decoders, all of which utilize the Maximum-a-Posteriori (MAP) algorithm. The MAP algorithm optimizes the error correction procedure, significantly reducing the number of iterations required for decoding transmitted information bits. The encoder side of the system utilizes a pseudorandom interleaver along with two recursive convolutional encoders. This method enhances the encoding procedure, thereby increasing the overall reliability and efficiency of Turbo codes within communication networks.

Keywords: Turbo Codes, Maximum-a-Posteriori Algorithm, Recursive Convolutional Encoders, Interleaver, VLSI Implementation, Error Correction.

1. INTRODUCTION

Currently, data transfer between systems is essential due to the continuous advancement of technologies and the simultaneous increase in the number of users. The extensive utilization of this technology results in significant challenges within digital communication systems, leading to data corruption. It is essential for telecommunications to minimize data corruption by implementing appropriate solutions to address errors that occur during the communication process. The Turbo algorithm is a method that decodes the process while simultaneously implementing effective corrections to the process. The Turbo algorithm is the most prominent method for decoding convolution codes. This algorithm can be implemented in both software and hardware configurations. Efficient data is presented by digital systems to facilitate well-organized communications. Data corruption represents a significant challenge faced by digital communication systems. To reduce data corruption, error-correcting codes represent an effective technique. Nearly all communication systems adopted this approach due to its efficient decoding capabilities; even the Turbo algorithm requires specific hardware configurations. During the decoding operation, existing functional obstructions can be mitigated, allowing for the implementation of an enhanced method known as the Adaptive Turbo Algorithm. The decoding of codes can be executed rapidly, as this algorithm demonstrates high efficiency in high-speed operations. Convolution codes are employed to achieve potential code sequences, utilizing the maximum-likelihood decoding process. This research primarily focuses on the significance of the Turbo algorithm in practical applications utilizing VHDL code. This research benefits students in communications as well as professionals in the field of decoders, serving as an efficient method for minimizing errors during advanced communication procedures. The Turbo algorithm is implemented using VHDL code to ensure accurate execution. The researcher selected VHDL code for this research due to its high capability in designing electronic systems, in addition to various other codes considered. In addition to students and business professionals, individuals can comprehend and evaluate the concepts of the Turbo algorithm, thereby enhancing their understanding of VHDL code and the associated tools

utilized in this research.

2.LITERATURE SURVEY

Akshaya, V., K. N. Sreehari, and Anu Chalil (2020)[1], proposed a Very Large Scale Integration (VLSI) architecture for the implementation of Turbo decoder. Soft-in-soft out decoders, interleavers and deinterleavers is used in the decoder side which employs Maximum-a-Posteriori (MAP) algorithm. The number of iterations required to decode the information bits being transmitted is reduced by the use of MAP algorithm. For the encoder part, this paper uses a system which contains two Recursive convolutional encoders along with pseudorandom interleaver in encoder side. The Turbo encoding and decoding is done using Octave, Xilinx Vivado, Cadence tools. The system is implemented and synthesized in Application Specific Integrated Circuit (ASIC).Timing analysis has been done and GDSII file has been generated.Zhan, Ming (2021)[2], proposed a reverse calculation based low memory turbo decoder architecture by partitioning the trellis diagram and simplifying the max* operator. The designed forward state metrics calculation architecture is merged with two classical decoding schemes. Through field programmable gate array (FPGA) hardware implementation, the state metrics cache (SMC) capacity is reduced by 65%, the power dissipation of the reverse calculation architecture is significantly reduced for all tested clock frequencies, and the decoding performance is not affected as compared with classical decoding schemes. The proposed reverse calculation architecture is an effective technique to achieve better decoding performance for power-constrained applicationsKumar, N.Sai Vamsi and G.Lakshmi Bharath (2020)[3], designed and implemented Turbo encoder to be an embedded module in the in-vehicle system (IVS) chip. Field programmable gate array (FPGA) is employed to develop the Turbo encoder module. Both serial and parallel computations for the encoding technique are studied. The two design methods are presented and analyzed. Developing the parallel computation method, it is shown that both chip size and processing time are improved. The logic utilization is enhanced by 73% and the processing time is reduced by 58%. The Turbo encoder module is designed, simulated, and synthesized using Xilinx tools. Xilinx Zynq-7000 is employed as an FPGA device to implement the developed module. The Turbo encoder module is designed to be a part of the IVS chip on a single programmable device. Weith offer, Stefan (2020)[4], presented recent findings on the implementation of ultra-high throughput Turbo decoders. They illustrated how functional parallelization at the iteration level can achieve a throughput of several hundred Gb/s in 28 nm technology. Our results show that, by spatially parallelizing the half-iteration stages of fully pipelined iteration unrolled decoders into X-windows of size 32, an area reduction of 40% can be achieved. We further evaluate the area savings through further reduction of the X-window size. Lastly, we show how the area complexity and the throughput of the fully pipelined iteration unrolled architecture scale to larger frame sizes. They considered the same target bit error rate performance for all frame sizes and highlight the direct correlation to area consumption. Paidmalla, Nagaraju, and Tummapala Lalitha Prasanna (2021) [5], designed and evaluated of area efficient pipelined turbo encoder and decoder is implemented. Turbo coding is very effective technique for correcting errors. These codes widely used in communication systems. Wireless communications (3G & 4G) includes turbo codes within it for accurate error correction. Earlier, the polar codes are implemented using 8 bits, so polar decoder is restricted by the inherent iterative process to compile the data at a higher rate. High decoding accuracy is the major flaw of polar coding implementation. Hence in this work, implementing 64-bit turbo encoder and decoder to compile the data at higher rate with reduced area and delay. The system is implemented and correlated in Application Specific Integrated Circuit (ASIC). At last compared with existed system, proposed system gives effective outcome in terms of delay and area.Rangachari, Sundarrajan, and Nitin Chandrachoodan (2020) [6], proposed a new state encoding mechanism as well as an organization of memory blocks that enables this power reduction, and quantify the effects. When combined with other schemes for early termination, the overall energy consumed per decoding operation can be reduced by between 10-20%. Ali, Amer T., and Dhafir Abdul Fatah Alneema (2020) [7] , proposed a new design of turbo decoder with one MAP decoder and it was designed with and without parallelism using different window technique in HLS tool which it is not explored previously. These designs were implemented for different frame size in this work. A comp-arison in latency and resource utilization where done and how a tradeoff done between these two parameters to reach the specific design that we need. The new design produces better results.Shrimali, Yanita, and Janki Ballabh Sharma (2021) [8] , proposed architecture, in order to achieve high throughput and low complexity, efficient Log-MAP turbo encoder/decoder and pipelined FFT processor is employed. Single delay feedback-based pipelined memoryless FFT/IFFT processor helps in achieving improved area and power efficiency, whereas high speed and good error correction capacity are obtained by Log-MAP turbo decoder. Simulation results obtained using Xilinx ISE Design suite are compared with state of the art architectures verifies the efficiency of the proposed system.Verma, Anuj, and Rahul Shrestha (2020) [9], proposed VLSI architecture of LDPC decoder processes quasi-cyclic LDPC encoded information which is received as log-likelihood ratios (LLRs) from soft demodulator at the receiver side. It achieved the adequate bit-error-rate (BER) of 10−6 between 2 to 4 dB of bit-energy to noise-power-spectral-density (Eb/N0) with 10 decoding iterations for various code rates like 1/3, 2/5, 1/2, 2/3, 3/4, 5/6, and 8/9. The VLSI architecture of 5G new-radio LDPC decoder has been field-programmable logic-array (FPGA) prototyped and its implementation results are compared with state-of the-art designs where

the proposed LDPC decoder shows lower hardware utilization up to 87%. To the best of our knowledge, this is the first VLSI-architecture of LDPC decoder reported for 5G new-radio compliant to the specifications of enhanced mobile broadband (eMBB).Le Gal, Bertrand, and Christophe Jego (2020) [10] , a new turbo decoder parallelization approach is proposed for x86 multi-core processors. It provides both: high-throughput and low-latency performances. In comparison with all CPU- and GPU-related works, the following results are observed: shorter processing latency, higher throughput, and lower energy consumption. Regarding to the best state-of-the-art x86 software implementations, 1.5 × to 2 × throughput improvements are reached, whereas a latency reduction of 50 × and an energy reduction of 2 × are observed.Dheeb, Khadija Omran, and Bayan Sabbar (2020) [11], presented an implementation of LTE turbo decoding using the Log- Maximum a posteriori (MAP) algorithm with reduced number of required cycles approximately by 75% based on serial to parallel operation. Additionally, an improvement for this algorithm based on polynomial regression function is done to reduce the implementation complexity. These system implementations, are designed with 40 bit block size of the input using Xilinx System Generator (XSG) to show its applicability in real time using two approaches; Hardware Co-Simulation and HDL Netlist based on three devices, Xilinx Kintex- 7, Spartan- 6 and Artix- 7.Boudaoud, Abdelghani, Mustapha El Haroussi, and ElhassaneAbdelmounim (2020) [12], presented the contribution of the insertion of a Turbo-type channel decoder in a MIMO chain. This MIMO chain is based on Orthogonal Space-Time Block Code (OSTBC). Alamouti proposed two structures, based on the OSTBC code and having two transmitting antennas: the first structure has a single receiving antenna, that is OSTBC 2 × 1 and the second one has two receiving antennas that is OSTBC 2 × 2. The turbo-decoder is based on the Difference Set Codes-One Step Majority Logic Decodable (DSC-OSMLD); it is the DSC (21, 11) code. After the introduction of this turbo decoder in the two Alamouti's structures, performance are noted and compared in terms of the Bit Error Rate (BER) versus the Signal-to-Noise Ratio (SNR). The obtained results show that the addition of a one receiving antenna to the 2 × 1 OSTBC structure provides a decoding gain equal to 1 dB, while the insertion of the proposed turbo decoder brings a gain of 5.5 dB at the first iteration only.

3. PROPOSED METHODOLOGY

Architecture of Turbo Coder Turbo encoder and decoder together comprises the Turbo coder architecture as shown in Figure 1. Two identical Recursive convolutional encoders (RSC) and a pseudorandom interleaver constitutes the turbo encoder as shown in Figure 2. The LTE employs a 1/3 rate parallel concatenated turbo code. Each RSC works on two different data. Original data is provided to the first encoder, while the second encoder receives the interleaved version of the input data. A specified algorithm is used to scramble the data bits and the method is called Interleaving. An appreciable impact on the performance of a decoder is seen with the interleaving algorithm when used. The RSC1 and RSC2 encoder outputs along with systematic input comprise the output of turbo encoder, that is, a 24-bit output is generated. This will be transmitted through the channel to the Turbo decoder. A standard turbo decoder block diagram is shown in Figure 3 that contains two modules of SISO decoders together with two pseudorandom interleavers and a pseudorandom deinterleaver.

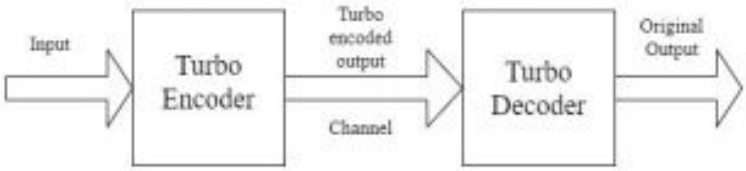

Figure 1 Proposed block diagram.

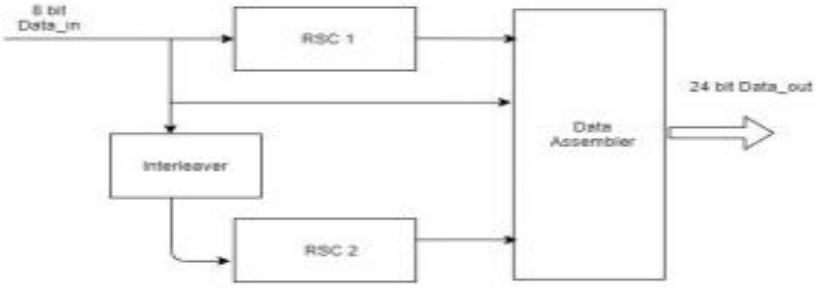

Figure 2. Turbo encoder operation.

The usually used method of turbo code decoding is carried out using the BCJR algorithm. The fundamental and basic idea behind the turbo decoding algorithm is the iteration between the two SISO part decoders which is illustrated in Figure 3. It comprises a pair of decoders, those which work simultaneously to refine and upgrade the estimate of the original information bits. The first and second SISO decoder, respectively, decodes the convolutional code generated by the first or second CE. A turbo-iteration corresponds to one pass of the first

component decoder which is followed by a pass of the second component decoder.

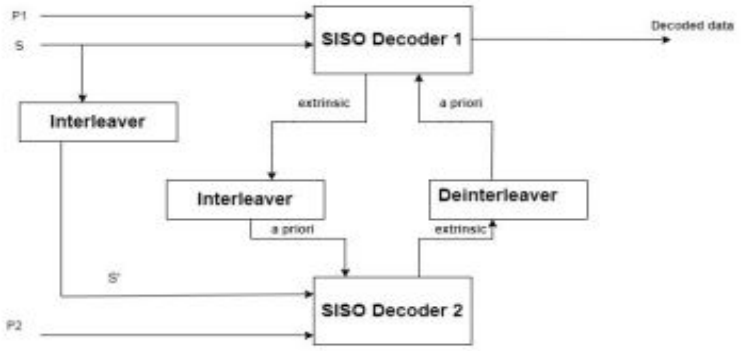

Figure 3. Turbo Decoder Block diagram

3.1 SISO Decoder

The signal which is received at the input of a soft-in-softout (SISO) decoder is the real (soft)value of that signal. An estimate of each input bit The decoder then generates an approximation for each data bit expressing the probability that the transmitted data bit is equal to one.The maximum a-posteriori (MAP) algorithm is used in the turbo-decoder under consideration in this paper for the SISO component decoder. The MAP algorithm never restricts the set of bit estimates to correspond strictly to a valid path through the trellis. Therefore, the results produced by a Viterbi decoder that recognizes the most likely true path through the trellis should differ from those generated by that. 1) The MAP Algorithm: The MAP algorithm minimizes the likelihood of bit error by using the entire sequence that was obtained to figure out the most likely bit at each trellis point. Consider a frame of N coded symbols consisting of m bits and the channel output received by the decoder as y. For every dsym i, a MAP decoder provides a 2m a posteriori probability.

3.2 Interleaver

Choosing the interleaver is a significant part of the turbo code design. Interleavers scramble data in a pseudorandom order to lessen the resemblance between adjacent bits at the input of the convolutional encoder. The interleaver is shown in Figure 4 is used on both the encoder part and the decoder part. It produces a long block of data on the encoder side, while it compares two SISO decoders' output in the decoder portion and helps to fix the error. Pseudo-random deinterleaver functions in a complimentary manner of pseudo-random interleaver.

4. RESULTS AND DISCUSSION

The simulation results will do by using in Vivado ISE. The timing, power and synthesis reports listed below.

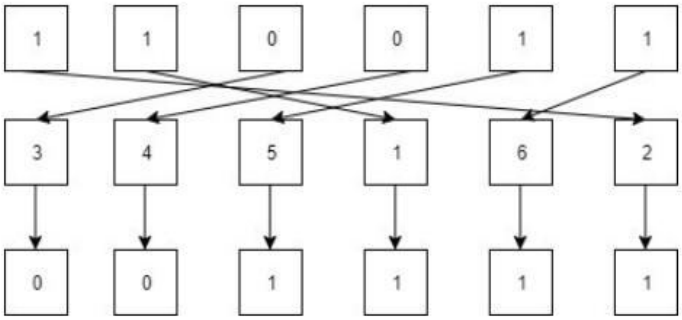

Figure 4. interleaver block diagram.

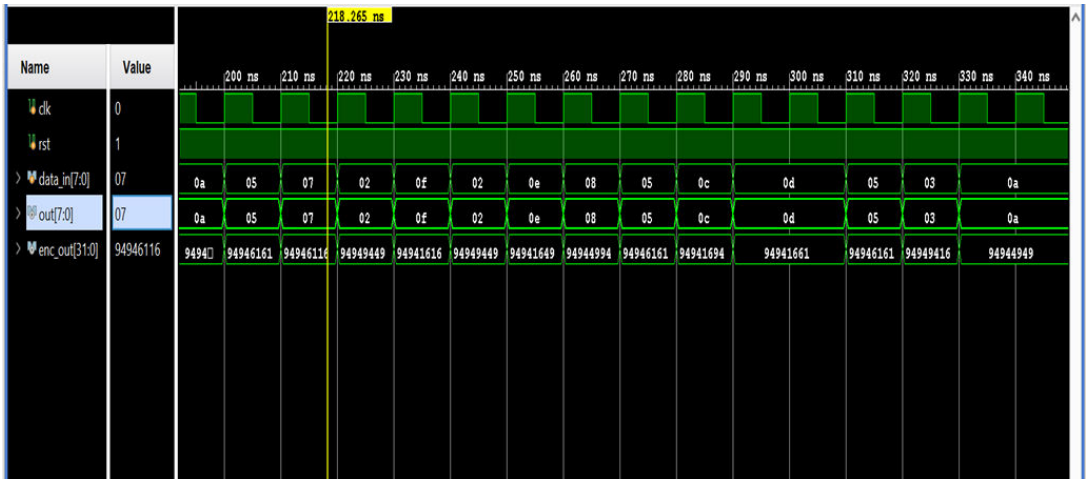

Figure 5. Simulation outcome

Resource	Utilization	Available	Utilization %
LUT	12	101400	0.01
IO	48	285	16.84

Figure 6 Design summary.

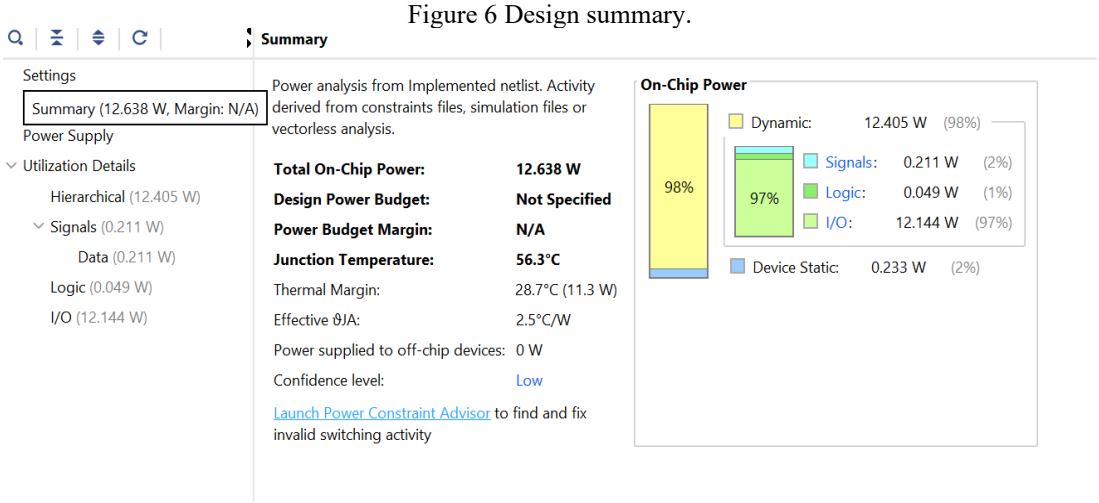

Figure 7. Power summary

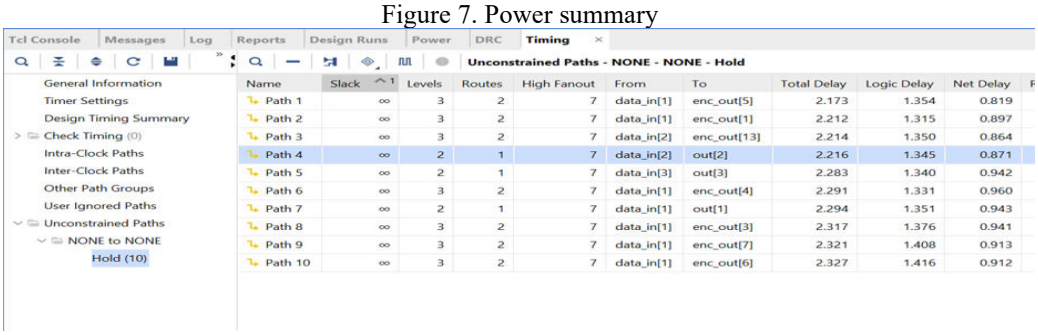

Figure 8. Time summary.

Table 1. Performance comparison.

Parameter	Hamming Code	Proposed Map Algorithm
Area (LUTS)	50	12
Power (Watts)	15.66	12.638
Delay (Ns)	3.50	2.30

5.CONCLUSION

Turbo algorithm is conceived more interesting and challenging for this research topic, it is considered, and it has wide variety of applications in digital communications field. This research helps to generate more profits by the developers using Turbo algorithm. Anyone besides students can easily analyze these Turbo algorithm concepts and can gain more knowledge about it. This research mainly concerned with implementation of Turbo algorithm using Verilog coding. Turbo algorithm has many advantages like low power consumption and main advantage is error correcting using Verilog. The main advantage of Turbo algorithm is the description will be low even in the presence of more errors and the algorithm works more effectively. Another advantage of using this Turbo algorithm is due to its cost effectiveness.

REFERENCES

[1] Akshaya, V., K. N. Sreehari, and Anu Chalil. "VLSI Implementation of Turbo Coder for LTE using Verilog HDL." 2020 Fourth International Conference on Computing Methodologies and Communication (ICCMC). IEEE, 2020.

[2] Zhan, Ming, et al. "Reverse calculation-based low memory turbo decoder for power constrained applications." IEEE Transactions on Circuits and Systems I: Regular Papers 68.6 (2021): 2688-2701.

[3] Kumar, N.Sai Vamsi and G.Lakshmi Bharath. "Designing of IVS chip encoder module in VLSI Architecture."(2020)

[4] Penchalaiah, Usthulamuri, and VG Siva Kumar. "Design and Implementation of Low Power and Area Efficient Architecture for High Performance ALU." Parallel Processing Letters 32.01n02 (2022): 2150017.

[5] S. V. G. Kumar, M. Vadivel, U. Penchalaiah, P. Ganesan and T. Somassoundaram, "Real Time Embedded System for Automobile Automation," 2019 IEEE International Conference on System, Computation, Automation and Networking (ICSCAN), Pondicherry, India, 2019, pp. 1-6, doi: 10.1109/ICSCAN.2019.8878820.

[6] Rangachari, Sundarrajan, and Nitin Chandrachoodan. "Energy Reduction in Turbo Decoding through Dynamically Varying Bit-Widths." 2020 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, 2020.

[7] Ali, Amer T., and Dhafir Abdul Fatah Alneema. "Design Analysis of Turbo Decoder Based on One MAP Decoder Using High Level Synthesis Tool." Al-Rafidain Engineering Journal (AREJ) 25.1 (2020): 70-77.

[8] Shrimali, Yanita, and Janki Ballabh Sharma. "Efficient HDL Implementation of Turbo Coded MIMO-OFDM Physical Layer." Nanoelectronics, Circuits and Communication Systems: Proceeding of NCCS 2019. Springer Singapore, 2021.

[9] Verma, Anuj, and Rahul Shrestha. "A new partially-parallel VLSI-architecture of quasi-cyclic LDPC decoder for 5G new-radio." 2020 33rd International Conference on VLSI Design and 2020 19th International Conference on Embedded Systems (VLSID). IEEE, 2020.

[10] Le Gal, Bertrand, and Christophe Jego. "Low-latency and high-throughput software turbo decoders on multi-core architectures." Annals of Telecommunications 75 (2020): 27-42.

[11] Dheeb, Khadija Omran, and Bayan Sabbar. "Different FPGA products based implementation of LTE turbo code." Iraqi Journal of Information and Communication Technology 3.1 (2020): 40-51.

[12] Boudaoud, Abdelghani, Mustapha El Haroussi, and ElhassaneAbdelmounim. "Turbo decoder based on DSC codes for multiple-antenna systems." Advanced Communication Systems and Information Security: Second International Conference, ACOSIS 2019, Marrakesh, Morocco, November 20–22, 2019, Revised Selected Papers 2. Springer International Publishing, 2020.