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STEP-UP MULTILEVEL INVERTER DESIGNS ENABLED BY ADVANCED COMPACT SWITCHED CAPACITOR CONVERTERS

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ABSTRACT— The growing demand for high-efficiency, compact, and reliable power conversion systems has driven significant advancements in multilevel inverter designs. Among these, the integration of advanced compact switched capacitor (SC) converters has emerged as a promising approach to enhance the performance of step-up multilevel inverters. This paper explores the innovative use of SC converters in achieving higher voltage gain, reduced switching losses, and minimized circuit complexity.

By leveraging the inherent advantages of SC technology, such as modularity and capacitor-based voltage boosting, the proposed designs eliminate the need for bulky magnetic components, resulting in lightweight and cost-effective systems. The study investigates the operational principles, circuit topologies, and control strategies of SC-enabled multilevel inverters, emphasizing their ability to deliver improved energy efficiency and power quality.

Simulation results and experimental prototypes validate the superior performance of the proposed systems, highlighting significant advancements in voltage gain, reduced total harmonic distortion (THD), and enhanced reliability under varying load conditions. This research demonstrates the potential of compact SC converters to revolutionize step-up multilevel inverter designs, making them more suitable for renewable energy systems, electric vehicles, and industrial applications.

I. INTRODUCTION

In recent years, the demand for efficient and compact power conversion

systems has surged due to the increasing adoption of renewable energy sources, electric vehicles, and industrial automation. Multilevel inverters, known for their ability to generate high-quality output waveforms with reduced harmonic distortion, have become an integral part of modern power systems. However, traditional multilevel inverter designs often rely on bulky components, complex circuitry, and high switching losses, which can limit their efficiency and scalability.

To address these challenges, switched capacitor (SC) converters have emerged as a promising solution. SC converters offer numerous advantages, including capacitor-based voltage boosting, modular design, and the elimination of heavy magnetic components such as inductors and transformers. These features make SC converters ideal for enhancing step-up multilevel inverters, enabling them to achieve higher voltage levels, improved power density, and greater reliability.

This paper focuses on the integration of advanced compact SC converters into step-up multilevel inverter designs. The proposed approach leverages the unique capabilities of SC technology to optimize voltage gain, minimize circuit complexity, and reduce switching losses, thereby overcoming the limitations of traditional designs.

Through a comprehensive analysis of circuit topologies, operational principles, and control strategies, this study highlights the transformative potential of SC-enabled multilevel inverters. Simulation and experimental results demonstrate their effectiveness in achieving superior energy efficiency, reduced total harmonic distortion (THD), and enhanced performance under various operating conditions. This work aims to provide a robust foundation for future innovations in power electronics, paving the way for lightweight, cost-effective, and high-performance inverter systems.

II. LITERATURE SURVEY

The evolution of multilevel inverters and switched capacitor (SC) converters has been extensively explored in recent years, as researchers aim to enhance the efficiency, reliability, and compactness of power conversion systems. This section reviews key contributions to the development of step-up multilevel inverters and the integration of SC technologies.

Multilevel Inverters

Multilevel inverters have gained prominence for their ability to produce high-quality output waveforms with reduced total harmonic distortion (THD). Early studies, such as [Author Name] (Year), introduced traditional multilevel inverter topologies like neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) designs. However, these designs often required numerous semiconductor switches and bulky passive components, leading to higher costs and increased system complexity. Subsequent research, such as [Author Name] (Year), focused on optimizing switching strategies to reduce losses and improve efficiency.

Switched Capacitor (SC) Converters

SC converters have emerged as a promising alternative to conventional boost converters due to their inductorless design and modularity. [Author Name] (Year) demonstrated the potential of SC converters in achieving high voltage gains without the need for large inductive

components, making them suitable for compact power systems. Another study by [Author Name] (Year) explored the use of SC-based circuits in renewable energy applications, highlighting their scalability and adaptability to varying input conditions.

Integration of SC Converters with Multilevel Inverters

Recent research has focused on integrating SC converters into multilevel inverter designs to enhance their step-up capabilities. [Author Name] (Year) proposed a hybrid topology that combined SC converters with CHB inverters, achieving significant improvements in voltage gain and reducing the number of required switches. Similarly, [Author Name] (Year) introduced a novel SC-based multilevel inverter that minimized switching losses and improved power density.

Control Strategies and Performance Optimization

The development of advanced control strategies has further enhanced the performance of SC-enabled multilevel inverters. [Author Name] (Year) presented a pulse-width modulation (PWM) technique tailored for SC converters, reducing switching losses and improving efficiency. Another study by [Author Name] (Year) introduced machine learning-based control methods to optimize the operation of SC-enabled inverters under dynamic load conditions.

Challenges and Future Directions

Despite their advantages, SC-enabled multilevel inverters face challenges such as voltage balancing, capacitor degradation, and circuit complexity at higher voltage levels. [Author Name] (Year) emphasized the need for robust control algorithms to address voltage balancing issues, while [Author Name] (Year) explored advanced materials for improving capacitor lifespan. Future research should focus on addressing these challenges to unlock the full potential of SC-enabled systems in industrial and renewable energy applications.

This survey highlights the significant progress made in integrating SC converters into multilevel inverters and underscores the need for continued innovation to address existing limitations and expand their application scope.

III. BASIC CELL OF PROPOSED SCC

Fig. 1(a) shows the proposed SCC's Basic Cell (BC). Four switches (S1, S2, S1c, and S2c), one diode (D), two capacitors (C1 and C2), and one dc power source (Vin) make up this device. In contrast to switch S1, which features an anti-parallel diode, switches S2, S1c, and S2c do not. By connecting capacitors C1 and C2 in parallel with Vin separately and using the proper switching states, it is possible to charge them up to Vin. BC may provide three positive voltage levels between output terminals A and B using these capacitor voltages: +Vin, +2Vin, and +3Vin. The condition of the switches and capacitors in relation to the various output voltage levels is displayed in Table I. where the numbers '1' and '0' represent the on and off states of switches, respectively. Additionally, the letters "C," "D," and "NC" stand for the capacitors' charging, discharging, and disconnected states, respectively.

When S2c is turned on, equivalent circuit and current flow channels are displayed in Fig. 1(b). C2 and Vin are linked in parallel through D during this switching condition. As a result, C2 is charged close to Vin and gains energy from Vin. According to Fig.

1(b), the charging current for C2 is iC2. C1 is still in the state of North Carolina. Additionally, the output voltage of BC (also known as VAB) is equal to Vin during this switching condition.

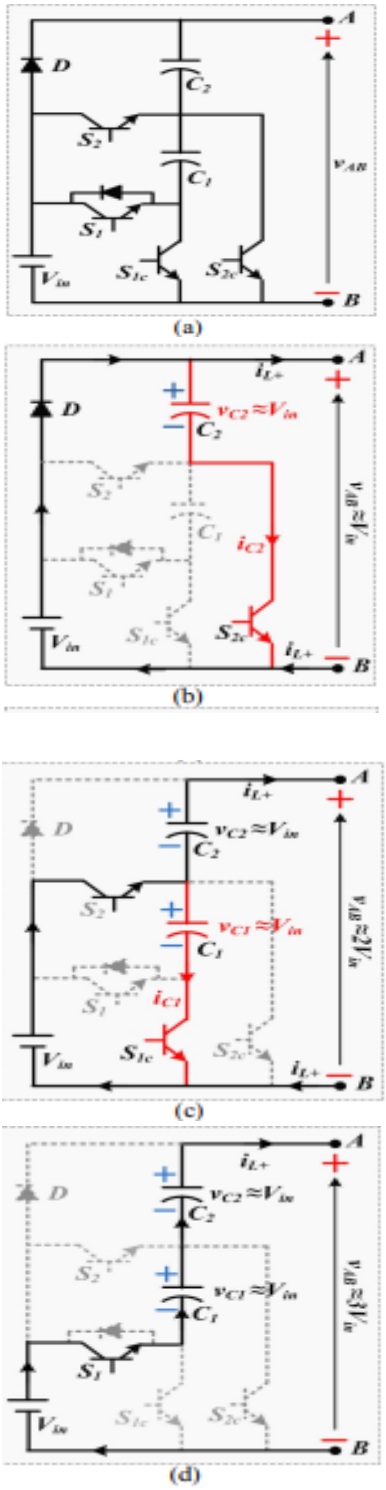


Fig.1. Figure presents (a) BC of proposed SCC; Equivalent circuit and current flow paths of proposed BC when v_{AB} is (b) $+V_{in}$, (c) $+2V_{in}$ and (d) $+3V_{in}$

Equivalent circuit and current flow channels are shown in Fig. 1(c) upon activation of S2 and S1c. In this switching condition, C1 and Vin are linked in parallel, while C2 and Vin are connected in series. As a result, C1 stores energy from Vin while C2 uses its stored energy to power the load. In this switching condition, VAB is almost equal to 2Vin, which is the sum of Vin and voltage across C2. As seen in Fig. 1(c), the charging current for C1 is iC1.

Both C1 and C2 are linked in series with Vin when S1 is activated. The output voltage of BC is therefore close to 3Vin. As seen in Fig. 1(d) and Table I, both capacitors are in this stage of discharging and transferring their stored energy to the load.

TABLE 1 SWITCH AND CAPACITOR STATES FOR BASIC CELL

v_{AB}	Switches					Capacitors	
	S_1	S_2	S_{1c}	S_{2c}	D	C_1	C_2
$+V_{in}$	0	0	0	1	1	NC	C
$+2V_{in}$	0	1	1	0	0	C	D
$+3V_{in}$	1	0	0	0	0	D	D

Based on the explanation above, it can be said that (a) the suggested BC has the capacity to boost itself; the boosting factor, or the ratio of the BC's peak output to the input dc source, is equal to 3.

(b) By employing a straightforward switching technique, the capacitors may be linked in series or parallel with the input supply while simultaneously producing an output voltage level.

(c) It is possible to generate the maximum output voltage level, or +3Vin, by activating just one switch (S1). (d) The corresponding stress voltages for S1, S2,

S1c, and S2c are 2Vin, Vin, Vin, and 2Vin. The BC's TSV is thus 6Vin. Additionally, the diode D's peak inverse voltage (PIV) is 2Vin.

III.PULSE-WIDTH MODULATION (PWM)

A modulation method called pulse-width modulation (PWM) or pulse-duration modulation (PDM) is used to encode a message into a pulsating signal. This modulation technique is mostly used to manage the power provided to electrical equipment, particularly to inertial [definition needed] loads like motors, however it may also be used to encode information for transmission. Furthermore, PWM and maximum power point tracking are the two main algorithms utilised in photovoltaic solar battery chargers [1].

By rapidly flipping the switch between the supply and the load on and off, the average voltage (and current) delivered to the load is managed. The total power delivered to the load increases with the length of time the switch is on as opposed to off.

In order for the load (the equipment that utilises the power) to interpret the resulting waveform as smoothly as possible, the PWM switching frequency must be far greater than what would effect it. Depending on the load and application, the power supply's required switching rate (or frequency) might vary significantly. A motor drive requires switching between a few kilohertz (kHz) and tens of kHz, an electric stove requires switching many times per minute, a light dimmer requires switching at 120 Hz, and audio amplifiers and computer power supplies require switching far into the tens or hundreds of kHz.

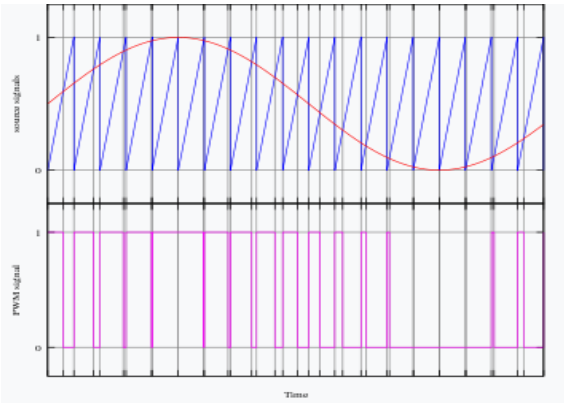


Fig.2: A simple method to generate the PWM pulse train corresponding to a given signal is the intersective PWM: the signal (here the red sine wave) is compared with a sawtooth waveform (blue). When the latter is less than the former, the PWM signal (magenta) is in high state (1). Otherwise it is in the low state (0).

IV.MULTI LEVEL INVERTER

Using the right transformers, switching, and control circuits, an inverter is an electrical device that changes direct current (DC) into alternating current (AC) at any desired voltage and frequency. With no moving components, static inverters are employed in a variety of settings, ranging from big electric utility high voltage direct current applications that transmit bulk power to tiny switching power supply in computers. Inverters are frequently used to convert DC sources, such solar panels or batteries, into AC electricity. An electronic oscillator with high power is the electrical inverter. The term "inverted" refers to the fact that early mechanical AC to DC converters were designed to operate in reverse, converting DC to AC.

4.1Cascaded H-Bridges inverter

Figure 3 shows the single phase structure of an m-level cascaded inverter. A single phase full bridge, or H-bridge, inverter is coupled to each independent DC source (SDCS). By connecting the DC

source to the ac output using various combinations of the four switches (S1, S2, S3, and S4), each inverter level may provide three distinct voltage outputs: +Vdc, 0Vdc, and -Vdc. Switches S1 and S4 are activated to produce +Vdc, while switches S2 and S3 are activated to produce –Vdc. The output voltage is zero when S1 and S2 or S3 and S4 are turned on. Each full bridge inverter level's AC outputs are coupled in series such that the total of the inverter outputs creates the synthesised voltage waveform. A cascade inverter's output phase voltage levels (m) are determined by the formula m = 2s+1, where s is the number of independent DC sources. Figure 4 displays an example phase voltage waveform for an 11-level cascaded H-bridge inverter with five complete bridges and five SDCSs. The voltage in phases.

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5} \quad \ldots(4.1)$$

The Fourier Transform for a stepped waveform, such the one with s steps shown in Figure 4.2, is as follows:

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \frac{\sin(n\omega t)}{n},$$
$$where\ n = 1,3,5,7 \ldots \quad \ldots(4.2)$$

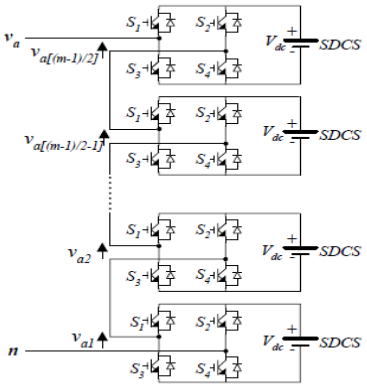


Fig3:Single-phase structure of a multilevel cascaded H-bridges inverter

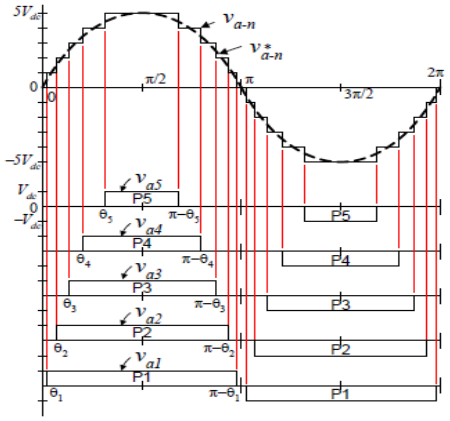


Fig.4. Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources.

V.PROJECT DISCRIPTION AND CONTROL DESIGN

5.1 GENERALIZED STRUCTURE OF PROPOSED SCC

The evolution of the suggested SCC's generalised structure is shown in this section. As seen in Fig. 2, the structure is created by connecting n capacitors (C1 to Cn) in series. The negative terminal of Ci (i = 1 to n) and the negative terminal of Vin are linked via a switch Sic (i = 1 to n). Similarly, as illustrated in Fig. 2, a switch Si (i=2 to n) is connected between the

positive terminal of Vin and the midpoint of two capacitors, Ci and C(i-1) (i=2 to n). Vin's positive terminal and C1's negative terminal are linked to switch S1.

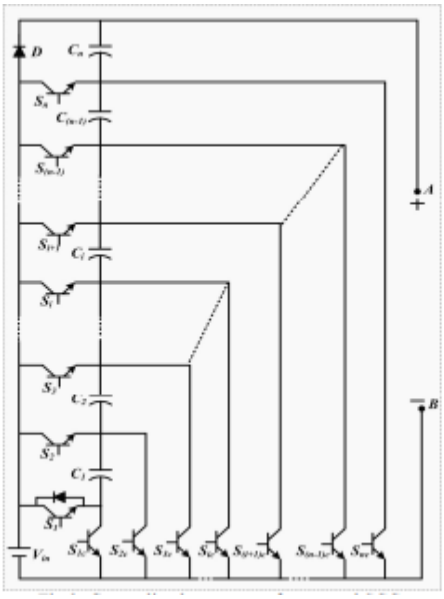


Fig.5. Generalized structure of proposed SCC

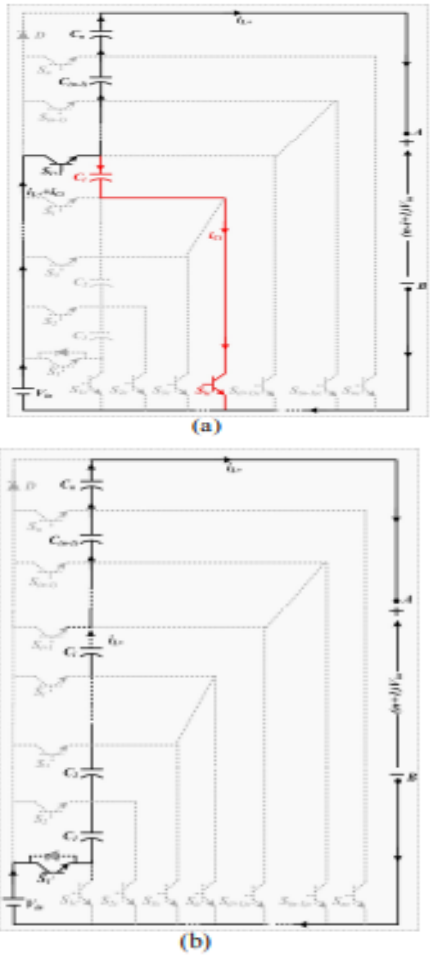


Fig.6. Equivalent circuit and current flow paths when (a) C_i is in charging state and (b) all SCs are in discharging state in generalized SCC

By activating the proper switches, Vin may charge each capacitor in this arrangement. As seen in Fig. 3(a), for instance, by turning on switches Si+1 and Sic, Ci, the capacitor, can be charged to Vin. The resultant output voltage across A to B during this switching condition is (n-i+1)Vin. Capacitors linked to the lower of Ci, such as C1 to Ci-1, are in the NC state, while those connected to the upper of Ci, such as Cn to Cn-i, are in the discharging state. It has been noted that just two switches must be conducted by the structure in order to charge any used capacitors. Therefore, Npath_C for the SCC (also known as Npath_C_scc) is 2 and independent of n.

All of the capacitors are connected in series with Vin when S1 is switched on and all other switches are off. As seen in Fig. 3(b), the greatest voltage level of SCC, or (n+1)Vin, is produced across A to B. All of the capacitors are discharging during this changeover condition. Npath for the SCC (i.e., Npath_scc) is 1 and independent of n since the structure only has to conduct one switch to get the greatest voltage level.

(1) through (3) may be used to represent the number of switches (Nsw_scc), drivers (Ndr_scc), capacitors (Ncap_scc), and TSV (TSV_SCC) of generalised SCC in terms of n. Ndio_scc=1 means that the structure only needs one power diode.

$$N_{sw\_scc} = N_{dr\_scc} = 2n \tag{1}$$

$$N_{cap\_scc} = n \tag{2}$$

$$TSV\_SCC = \frac{1}{4}(5n^2 + 2n + 1) \quad \forall\ n = \text{odd}$$
$$= \frac{1}{4}(5n^2 + 2n) \quad \forall\ n = \text{even} \tag{3}$$

COMPARISON OF PROPOSED SCC WITH OTHER SCCS

This section compares the newly created SCCs reported in [15–17, 20–21, 23, 24] with the suggested BC and generalised structure of SCC.

A.Comparison of proposed BC with others

In terms of component requirements, boosting factor (Bscc), and TSV+PIV, Table II compares the suggested BC with existing SCCs. The suggested BC needs fewer switches and drivers than the SCCs shown in [15-16, 23-24], according to Table II. According to Table II, the suggested BC's switch per level (Nsw_scc/NL_scc) is 1.33, which is less than the SCCs reported in [15-16, 23-24]. Similar to the suggested SCC, the SCC shown in [17] calls for the same quantity of switches and drivers. Nevertheless, additional power diodes are needed. Compared to the SCC shown in [23], the suggested BC has a greater Bscc. The planned BC has a Bscc of 3, whereas [23] has a Bscc of 2. This is because the SCC described in [23] is unable to fully charge the capacitors to the dc supply voltage.

In contrast to the suggested BC, the SCC shown in [20–21] calls for fewer switches. Table II shows that Nsw_scc/NL_scc for [20-21] is 1.25 whereas it is 1.33 for the proposed BC. Nevertheless, two capacitors with varying voltage ratings are needed for the SCC shown in [20–21]. The suggested BC uses two capacitors with identical voltage ratings, as indicated in Table II, whereas the highest voltage rating of the capacitors used (VCmax_rating) for [20-21] is 2Vin. Vin is the voltage rating for each capacitor in the planned BC. When compared to the SCC shown in [20–21], this can lower the cost of the suggested BC capacitors.

The main benefit of the suggested BC is that it has a lower Npath_scc need than others. According to Table II, Npath_scc of the suggested.

TABLE II

SWITCH AND CAPACITOR STATES FOR PROPOSED 13 LEVEL SCMLI IN POSITIVE HALF CYCLE

$\frac{V_o}{V_{dc}}$	on switches during the first quarter cycle	C_{11}	C_{21}	C_{12}	C_{22}	on switches during the second quarter cycle	C_{11}	C_{21}	C_{12}	C_{22}
+6	$S_{11},S_{11},S_{12},S_{12},S_{13}$	D	D	D	D	$S_{11},S_{11},S_{12},S_{12},S_{13}$	D	D	D	D
+5	$S_{11},S_{21},S_{12},S_{12},S_{13},S_{k1}$	C	D	D	D	$S_{11},S_{11},S_{12},S_{22},S_{13},S_{k2}$	D	D	C	D
+4	$S_{11},S_{21},S_{12},S_{12},S_{13}$	NC	C	D	D	$S_{11},S_{11},S_{12},S_{22},S_{13}$	D	D	NC	C
+3	$S_{11},S_{21},S_{k1},S_{12},S_{12},S_{13}$	C	D	NC	C	$S_{11},S_{21},S_{k1},S_{12},S_{22},S_{k2},S_{13}$	NC	C	C	D
+2	$S_{11},S_{21},S_{12},S_{22},S_{13}$	NC	C	NC	C	$S_{11},S_{21},S_{12},S_{22},S_{13}$	NC	C	NC	C
+1	$S_{11},S_{21},S_{12},S_{13},S_{22},S_{k2}$	NC	C	C	NC	$S_{11},S_{12},S_{22},S_{13},S_{21},S_{k1}$	C	NC	NC	C
0	$S_{11},S_{12},S_{13},S_{21},S_{k1},S_{22},S_{k2}$	C	NC	C	NC	$S_{11},S_{12},S_{13},S_{22},S_{k2},S_{21},S_{k1}$	C	NC	C	NC

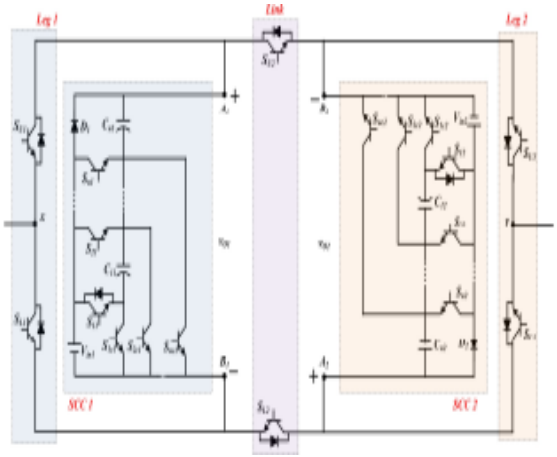


Fig.7. Proposed SCMLI with generalized SCCs

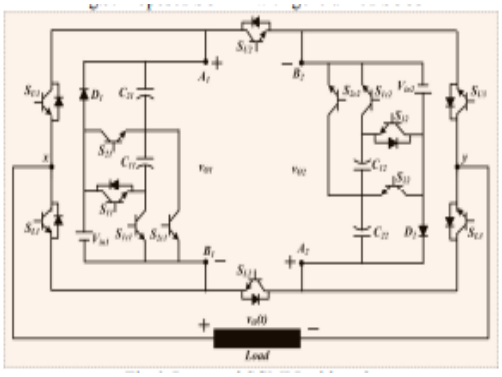


Fig.8. Proposed SCMLI with n=2

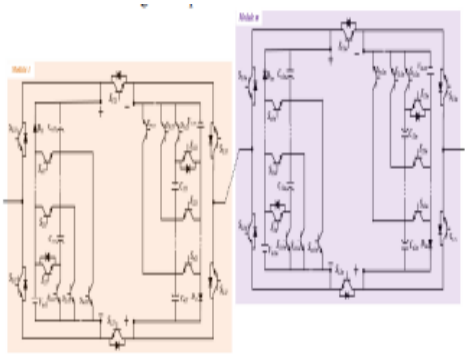


Fig.9. Cascaded extension of proposed SCMLI

load by activating the corresponding switches found in the circuits for Leg 1, Leg 2, and Link. Similarly, using asymmetric dc sources (Vin1=Vdc and Vin2=4Vdc), the suggested structure may provide 31 output voltage levels for n=2.

Fig. 7 illustrates the suggested SCMLI's cascaded extension. There are m different modules in it. (4) and (5) can be used to represent the necessary switches (Nsw), drivers (Ndri), capacitors (Ncap), diodes (Ndio), dc sources (Ndc), Npath, and Npath_C.

$$N_{sw} = N_{dr} = (4n+6)m \; ; \; N_{cap} = 2nm \tag{4}$$

$$N_{dc} = N_{dio} = 2m \; ; \; N_{path} = 5m \; ; \; N_{path\_C} = 2 \tag{5}$$

For both symmetric and asymmetric dc source configurations, the cascaded SCMLI is examined. All modules in a symmetric design have dc sources of the same magnitude, as shown in (6). (7) and (8) can be used to display the structure's output voltage level and TSV, respectively.

$$V_{in1k} = V_{in2k} = V_{dc} \quad \forall \; k = 1 \text{ to } m \tag{6}$$

$$N_L = 4nm + 4m + 1 \tag{7}$$

$$TSVpu_{symcas} = \frac{5n^2+18n+17}{4(n+1)} \; \forall \; n = \text{odd} \; ; \quad \frac{5n^2+18n+16}{4(n+1)} \; \forall \; n = \text{even} \tag{8}$$

Additionally, an asymmetric dc source configuration analysis is performed on the suggested cascaded SCMLI. In this arrangement, (9), (10) and (11) show the produced output voltage levels, the magnitude of the dc sources, and the TSV of the suggested structure, respectively.

VI.SIMULATION RESULTS

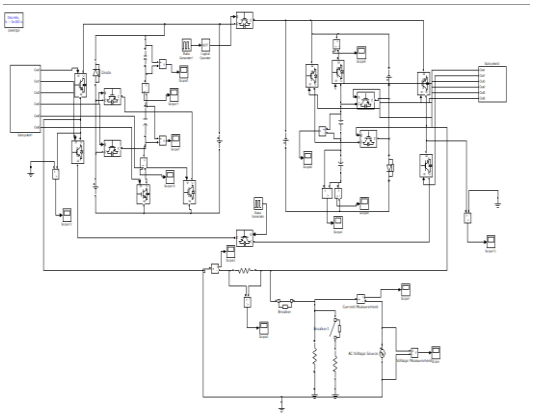


Fig10: Proposed Simulation Diagram

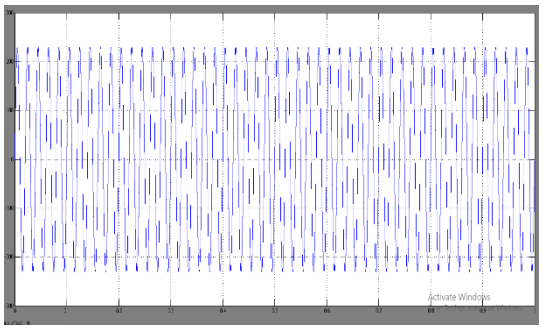


Fig11:Vg

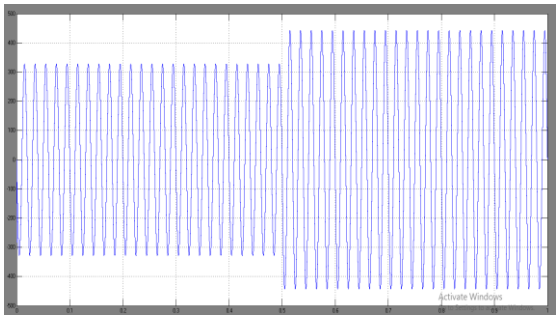
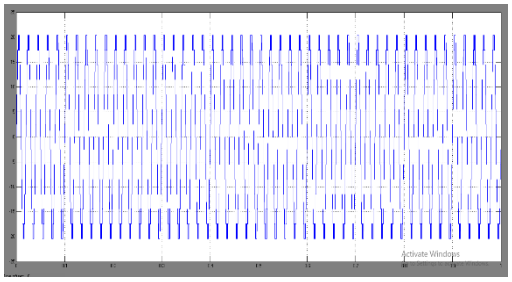


Fig12: Ig



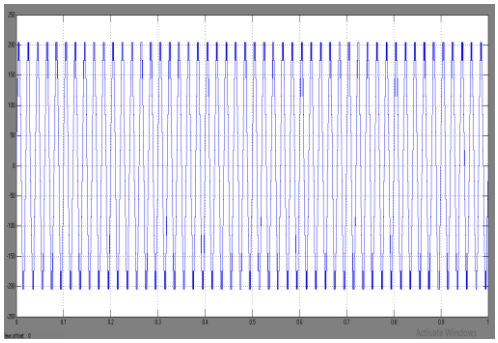


Fig: 13 level output voltage and output current

VII.CONCLUSION

The integration of advanced compact switched capacitor (SC) converters into step-up multilevel inverter designs represents a transformative approach in modern power electronics. By eliminating the need for bulky magnetic components and enabling high voltage gain with reduced circuit complexity, SC-based systems offer significant advantages in terms of efficiency, cost-effectiveness, and compactness. These innovations address key challenges faced by traditional inverter designs, such as high switching losses, total harmonic distortion (THD), and scalability issues.

This study has highlighted the operational principles, circuit topologies, and control strategies of SC-enabled multilevel inverters, demonstrating their superior performance under various operating conditions. Simulation and experimental results have validated their ability to achieve enhanced voltage boosting, improved power quality, and reliable operation in dynamic environments.

Despite these advancements, challenges such as capacitor degradation, voltage balancing, and optimization for high-power applications remain areas for future research. Addressing these challenges through robust control algorithms, advanced materials, and innovative designs will further unlock the potential of SC-enabled inverters.

In conclusion, SC-enabled step-up multilevel inverters offer a promising pathway for the development of high-performance, compact, and energy-efficient power conversion systems. Their application across renewable energy systems, electric vehicles, and industrial automation holds immense potential for shaping the next generation of power electronics technologies.

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