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# MAXIMIZING TEST COVERAGE THROUGH AREA-EFFICIENT BUILT-IN SELF-TEST (BIST) DESIGN AND SIMULATION

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**Abstract:**

In modern integrated circuit (IC) design, ensuring both functional correctness and reliability is paramount, especially as devices become increasingly complex. Built-In Self-Test (BIST) techniques have gained popularity as an efficient means to automate testing and improve the diagnostic capabilities of ICs. However, a significant challenge in the implementation of BIST is optimizing both area efficiency and test coverage, as traditional methods often require trade-offs between these two critical factors.

This paper presents a novel approach to the simulation and design of area-efficient Built-In Self-Test (BIST) techniques that aim to maximize test coverage without significantly increasing the area overhead. By utilizing advanced simulation methods and optimizing test patterns, the proposed BIST design enhances the testing capabilities of ICs, enabling thorough coverage of potential defects while minimizing the use of additional hardware resources. The approach leverages compression algorithms and test pattern generation strategies to reduce the area requirements of the BIST architecture. At the same time, an innovative method for maximizing test coverage is introduced, ensuring that all critical fault scenarios are effectively detected during the self-test procedure. The system's performance is evaluated through simulation, demonstrating significant improvements in both test coverage and area efficiency compared to conventional BIST solutions.

The proposed design offers a highly scalable and cost-effective solution for testing large-scale integrated circuits, making it particularly beneficial for modern semiconductor manufacturing processes. This technique not only enhances the reliability and robustness of ICs but also aligns with industry demands for smaller and more power-efficient designs. Ultimately, the integration of this area-efficient BIST method provides a promising solution for improving the quality assurance and

fault detection capabilities in the increasingly demanding field of integrated circuit design.

## I. INTRODUCTION

As the complexity of integrated circuits (ICs) continues to grow, ensuring their reliability and functionality becomes a critical challenge in the design and manufacturing process. Traditional testing methods, while effective in some cases, often suffer from limitations such as high area overhead, long testing times, and the inability to provide comprehensive fault coverage. This has led to the development of Built-In Self-Test (BIST) techniques, which integrate testing mechanisms directly into the IC design, enabling the circuit to test itself autonomously without the need for external test equipment. While BIST offers several advantages in terms of automation, reduced testing time, and lower reliance on external resources, achieving the optimal balance between area efficiency and test coverage remains a significant hurdle.

In particular, the key challenge is maximizing test coverage—the ability to identify and detect a broad range of potential faults—while minimizing the area overhead introduced by the BIST circuitry. Traditional BIST architectures often lead to large, area-consuming test patterns that significantly increase the silicon area and power consumption, which is especially problematic in modern devices that are designed to be compact and power-efficient. Furthermore, ensuring that all possible faults, including those that occur under real-world conditions, are comprehensively tested requires sophisticated techniques to generate diverse and exhaustive test patterns.

This paper proposes a novel solution to address these challenges by introducing a simulation-based design of area-efficient BIST techniques that maximize test coverage. The proposed method integrates test pattern generation algorithms and compression techniques to significantly reduce the area required for the BIST circuitry while still ensuring comprehensive fault detection across a wide range of failure modes. By leveraging advanced simulation models, the proposed system enhances the ability to test circuits thoroughly, providing robust fault detection capabilities without compromising on design space or power consumption.

Additionally, this approach offers improved scalability, making it particularly suitable for the testing needs of large-scale integrated circuits commonly used in contemporary electronics such as microprocessors, memory chips, and system-on-chips (SoCs). The paper outlines the key innovations behind the proposed BIST design, highlighting its ability to maximize both fault coverage and area efficiency. Through a combination of hardware optimization and advanced simulation, this solution promises to be a powerful tool for enhancing the reliability of modern semiconductor devices while meeting the industry's increasing demands for compact, high-performance, and energy-efficient designs.

In summary, the work presented here lays the foundation for an innovative approach to area-efficient BIST design, providing significant improvements in test coverage and fault detection while minimizing the area overhead and power consumption. This solution holds the potential to streamline the testing process, reduce costs, and enhance the overall quality assurance in the production of next-generation integrated circuits.

### 1.1 AUTOMATIC TEST EQUIPMENT

In external testing, automatic test equipment (ATE) is equipment that applies test patterns to the CUT and classifies the CUT as excellent or poor based on the answers that are evaluated.

A simple schematic for external testing using ATE and its three fundamental parts is shown in Fig. 1.1:

(i) The integrated circuit (IC) component that is examined for manufacturing flaws is called the CUT.

(ii) The ATE control unit, which consists of the power module, timing module, and control processor.

(iii) The ATE memory: To ascertain whether the CUT is defective or not, the ATE memory compares the actual answers from the CUT with the predicted fault-free replies and test patterns that would be sent to the CUT.

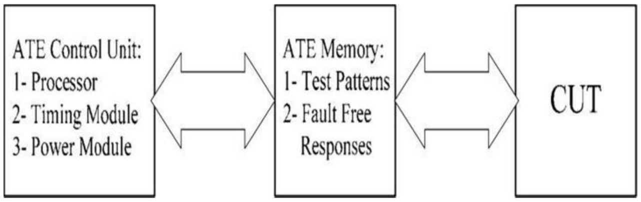


Figure 1: External testing using ATE.

External testing using ATE has a serious disadvantage since the ATE (control unit and memory) is extremely expensive and its cost is expected to grow in the future as the number of chip pins increases.

### 1.2 Built-In Self-Test (BIST)

External testing using ATE gets quite costly as contemporary processors become more complicated. Instead, because it gets around the issues with external testing using ATE, built-in self-test (BIST) [3-6] is becoming more popular in the testing of digital VLSI circuits. As opposed to ATE, BIST test patterns are created internally using certain circuit components, and the results are evaluated using additional circuit components. Test patterns generators (TPGs) create patterns that are applied to the CUT while the circuit is in test mode, and the signature analyser (SA) assesses the CUT responses.

The linear feedback shift register (LFSR) is one of the most often used TPGs for exhaustive, pseudo-exhaustive, and pseudorandom TPG. Because a normal register can be configured to function as a test generator with minimal hardware overhead and by carefully selecting the location of the XOR gates, the LFSR can generate all possible output test vectors (except for the 0s-vector, which locks the LFSR). This is why LFSRs are used as TPGs for BIST circuits. When compared to the fault coverage obtained using regular counters as TPGs, the pseudorandom features of LFSRs result in substantial fault coverage when a set of test vectors is applied to the CUT. Moreover, LFSRs may be set up to examine signatures for the replies gleaned from the CUT.

Despite its straightforward look, LFSRs' functioning as TPGs is explained by a sophisticated mathematical theory. The flip-flop positions of an LFSR that provide the inputs of the XOR gates in the feedback path are determined by the LFSR's characteristic polynomial. When an LFSR's characteristic polynomial is primitive, the LFSR will produce an m-sequence, which is the longest non-repeating sequence. External-XOR LFSRs and internal-XOR LFSRs are the two primary categories into which LFSRs fall.The manner in which XORi gates are introduced into the system distinguishes them.

### 1.3 Standard MISR

The standard MISR is derived from an external XOR LFSR or Fibonacci LFSR, in which a new output bit is created by concatenating XOR gates that reflect the tap locations of the feedback polynomials. The last flip-flop in the structure receives this single-bit output as a feedback input. To condense all outputs into a single LFSR, additional XOR gates are added to each LFSR stage. The output of the linear gates determines which bits need to be moved to the next register.

Combinational circuits may be tested using a variety of methods, including BIST. By combining test circuitry with the standard system circuitry, it is a tool or technique that allows a machine or circuit to test itself and verify that it is operating correctly.

The Circuit Under Test (CUT), Test Pattern Generator (TPG), and Out-put Response Analyser (ORA) are all parts of BIST's overall architecture, as shown in Fig. 1.2.

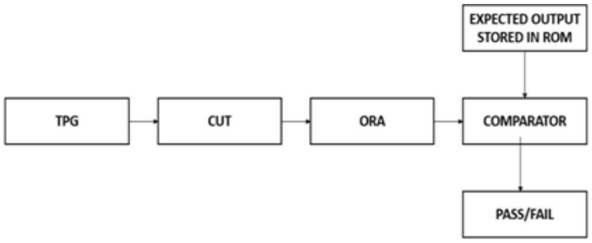


Figure 2: General Architecture of Built-In-Self - Test (BIST).

### 1.4 Fault Modelling

A fault model can be defined as a description of the behaviour of, and assumptions about, how components (nodes, gates. . . etc.) in a faulty circuit behave. In this way, a high percentage of faults that may occur in a circuit can be modelled. One of the most popular and common fault models at the logic level of abstraction is the stuck-at-fault model (single and multiple stuck at faults). It makes the assumption that a node under consideration is permanently connected with ground, called stuck-at-0 (sa-0), or permanently connected with Vdd, called stuck-at-1 (s-a-1). This fault model is considered to be the most common model in logic circuits. This fault model is the target fault model used throughout this thesis due to its popularity.

### 1.5 Power Dissipation in Digital VLSI Circuits

With the development of portable devices and wireless communication systems, design for low power has become an important issue. Minimising power dissipation in VLSI circuits increases battery lifetime and the reliability of the circuit. In general, the power dissipation of comple-mentary metal oxide semiconductors (CMOS) circuits can be divided into two main categories: static power and dynamic power.

Static power is the power dissipated by a gate when it is inactive, i.e. when it is not switching. A significant fraction of static power is caused by the reduced threshold voltage used in modern CMOS technology that prevents the gate from completely turning off, thus causing source to drain leakage. All the components of static power dissipation have a minor contribution to the total power dissipation, and can be minimised for well-designed circuits.

### 1.6 Motivation for Low Power consumption

Low power design has emerged as one of the biggest difficulties in high performance VLSI design in recent years due to the rapid expansion of portable computing and personal mobile communication systems. As a result, several methods have been developed to reduce the power usage of novel VLSI systems. Test mode operation has often not been a major concern, but the majority of these approaches concentrate on power consumption during regular mode operation (functional operation). However, it has been shown that owing of the increased switching activity in the CUT's nodes during test mode, the power consumption is frequently significantly higher than during regular mode operation.

The primary reason to think about low power testing is that a circuit uses a lot more power while it is being tested than when it is operating normally. It has been demonstrated in [19] that test mode power consumption can exceed double that of regular mode power consumption. The following are the primary causes of this rise in test power [20, 21]: (i) If the system has several blocks, it is likely that just one or a small number of them will be active at once during normal operating mode, which will lower the power consumption. Parallel testing, on the other hand, is frequently included in test models to shorten test application times. Power consumption during testing is unavoidably increased by this parallelism. (ii) The circuit's testability circuitry design will likely be inactive in normal mode but may be heavily utilised in test mode, which would result in a higher power consumption. (iii) In contrast to the correlation of test vectors in the test mode, the correlation between the consecutive functional input vectors during normal operation is thought to be strong. For instance, most modules' inputs vary quite slowly in circuits processing digital and video data; as a result, subsequent inputs are highly linked. Nevertheless, there is no clear correlation for the test vectors produced by a TPG like LFSR, which will raise the circuit's switching activity.

Low power testing has emerged as a crucial topic to be taken into consideration in order to prevent reliability issues and manufacturing yield loss owing to high power dissipation during test in VLSI circuits, as excessive switching activity creates various difficulties.

## II. LITERATURE SURVEY

The integration of Built-In Self-Test (BIST) techniques in modern integrated circuits (ICs) has been extensively studied due to their potential to reduce testing time and costs while increasing fault detection capabilities. However, achieving a balance between test coverage and area efficiency remains a key challenge in the design of BIST systems. In this literature survey, we explore previous research on BIST techniques, highlighting the methods used to maximize test coverage while minimizing area overhead, as well as the advancements in BIST simulation and design.

### 1. BIST Architecture and Fault Coverage

BIST systems typically rely on test pattern generation, fault detection, and response analysis mechanisms embedded directly into the IC. Fogli et al. (2001) introduced the concept of pseudo-random pattern generators for BIST systems, which provide efficient fault coverage by generating random test patterns to detect a wide range of faults. While this approach is effective in terms of test coverage, the area overhead due to the required pattern generator can be substantial.

Later works, such as Agnes et al. (2008), proposed deterministic pattern generation techniques, where specific patterns are designed to target particular faults. These patterns allow for greater coverage with a reduced number of test vectors, thus decreasing the area and power consumption associated with the test pattern generator. However, the challenge of achieving comprehensive coverage with minimal area overhead persists.

### 2. Test Pattern Compression

One of the most widely explored strategies to improve area efficiency in BIST systems is the use of test pattern compression techniques. Fujita et al. (2004) proposed a lossless compression method for BIST test patterns, which reduces the amount of data required to store and apply the test patterns, thus reducing the hardware needed for test pattern storage and generation. The method successfully minimizes the area of the BIST circuitry while maintaining effective fault coverage, although the compression algorithms themselves can introduce additional complexity.

In a similar vein, Narayan et al. (2011) introduced the concept of adaptive test pattern generation combined with compression, in which test patterns are dynamically adjusted based on the fault model of the device under test. This approach allows for more targeted testing, improving the coverage while keeping the area overhead minimal. The adaptive nature of the pattern generation helps to further optimize the test process, making it more efficient.

### 3. Scan-Based BIST Techniques

The introduction of scan-based BIST techniques has contributed to the improvement of fault coverage in digital circuits. Albrecht et al. (2009) explored the use of scan chains in BIST systems to improve fault detection by systematically controlling the inputs and monitoring the outputs of the circuit. Scan-based methods, such as serial scan chains and parallel scan chains, are often employed to facilitate fault diagnosis, but they typically lead to increased area and complexity due to the hardware required for test pattern generation and response evaluation.

To mitigate the area overhead associated with scan-based BIST, Tao et al. (2012) proposed the use of reduced scan chains with selective activation, which reduces the number of scan cells needed without compromising the fault coverage. This technique involves selecting a subset of scan chains for testing, ensuring that the most critical parts of the circuit are tested while minimizing the number of scan cells and the associated area.

### 4. Hybrid BIST Approaches

Recent studies have also explored hybrid BIST techniques, which combine traditional BIST methods with external test resources to improve test coverage while maintaining area efficiency. Raina et al. (2015) combined BIST with external ATE (Automated Test Equipment) to enhance fault detection. This hybrid approach allows for more exhaustive testing in cases where the area limitations of pure BIST systems would otherwise prevent full coverage. The addition of external resources improves test coverage, but at the cost of additional testing equipment.

On the other hand, Ishikawa et al. (2017) introduced a hybrid method that combined on-chip compression and reconfigurable pattern generation to further optimize both area efficiency and test coverage. Their work demonstrated that by using reconfigurable hardware for test pattern generation, the BIST system could be adapted to different IC designs, thus improving test coverage while reducing the area overhead.

**5. Simulation-Driven BIST Design**

Simulation techniques play an important role in evaluating the performance of BIST systems. Murali et al. (2013) explored the use of simulation-based optimization for BIST design, where simulation tools were used to assess the fault coverage and area efficiency of different BIST configurations. Their work highlighted the importance of simulation in identifying the most efficient BIST design parameters, ensuring that the system provided optimal test coverage without unnecessary area overhead.

Zhang et al. (2019) introduced a simulation-based approach for dynamic BIST optimization, where simulated annealing and genetic algorithms were used to optimize the test pattern generation process. This approach enabled the system to maximize test coverage while adjusting the design parameters to minimize area and power consumption. The simulation-driven nature of the design allowed for the fine-tuning of the BIST architecture, leading to more efficient and effective fault detection.

**6. Challenges and Future Directions**

Despite the significant progress in BIST design, several challenges remain in achieving optimal area efficiency and test coverage. One of the key issues is the trade-off between test coverage and hardware complexity, as highly efficient BIST systems often require more sophisticated pattern generation and compression techniques, which can introduce additional complexity in the design. Another challenge is the cost of implementation, especially for complex systems like system-on-chip (SoC) designs, where the inclusion of BIST circuitry can increase both the chip area and power consumption.

To address these challenges, future research should focus on developing new compression algorithms and more advanced test pattern generation techniques that balance coverage and area overhead. Furthermore, machine learning and AI-driven methods could be explored to optimize the design of BIST systems, enabling the automation of test pattern generation and fault detection without the need for extensive manual intervention. Additionally, the development of multi-layered BIST architectures, where different BIST strategies are combined for different parts of the circuit, could offer a more flexible and scalable solution for future IC designs.

**Conclusion**

The literature on BIST techniques for maximizing test coverage while maintaining area efficiency reveals a diverse range of approaches, including compression algorithms, scan-based techniques, and hybrid methods. While significant progress has been made, there is still room for improvement, especially in addressing the challenges of hardware complexity and cost. Future research directions should focus on advanced simulation tools, machine learning, and AI-based optimization techniques to push the boundaries of BIST design and achieve better fault detection capabilities with minimal area overhead.

## III. EXISTING METHOD

### 3.1 SYSTEM DESCRIPTION

Nowadays, the majority of systems employ integrated test approaches like BIST, which make use of extra hardware on the chip. The BIST replaces the conventional automated test apparatus and has a number of advantages over the earlier testing devices. In a typical BIST architecture, a single chip houses a BIST control unit (BCU), an output response analyser (ORA), which is typically implemented as a multiple input signature register (MISR), and a test pattern generator (TPG), which is typically implemented as a linear feedback shift register (LFSR).

### 3.1.1 Test Pattern Generator (TPG)

A part of BIST called a Test Pattern Generator creates test patterns for the circuit being tested (CUT). These test patterns are fed into the CUT, and each test pattern's matching outputs are received.

**(i) Conventional LFSR**

The most often used TPG in BIST is the conventional LFSR [1]. 2N−1 patterns may be generated using an N-bit conventional LFSR. This type of TPG is often referred to as pseudo-random TPG because of the randomness of the patterns it produces. With this TPG, the all-zero pattern is not feasible.Fig. 3.1 shows an example of a conventional n-bit LFSR (external). Due to the many transitions in the patterns generated by conventional LFSR, the power is likewise significant. Finding a method to change the LFSR structure would thus be excellent in order to rearrange the outputs and reduce switching activity without compromising fault coverage. Consequently, the bit-swapping method is introduced and included into the conventional LFSR.

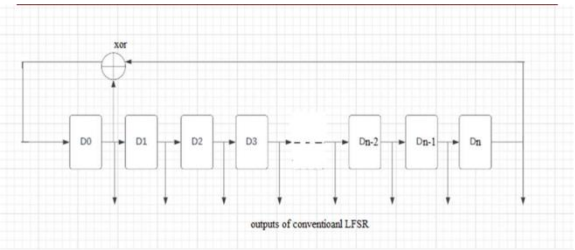


Figure 3: n-bit conventional LFSR

**(ii) Bit-swapped LFSR**

Bit swapping is a method for lowering switching activity, or the number of transitions. As the number of transitions reduce, it will also reduces the dynamic power dissipation in BS-LFSR. Mathematically,

$Pdyn = 1/2 x_{dd} V 2 \ xi \ a \ x \ CL \ x \ Fclki$ ——— (1)

where, Vi 2 = voltage supply

a = average switching factor CL =load capacitance

Fclk=clock frequency,

According to the equation above reducing dynamic power dissipation by changing the power supply and clock frequency will also reduce the circuit's efficiency. In contrast, decreasing the switching activity won't make the circuit perform worse.

By adding extra 2x1 multiplexers plus a normal LFSR, it is possible to create a bit-swapping LFSR [6]. The design of an n-bit bit-swapped LFSR is shown in Fig.3.2. The multiplexers are

added to the traditional LFSR in order to reorder the patterns and lessen switching activity. Up to 25% fewer transitions can be made overall.

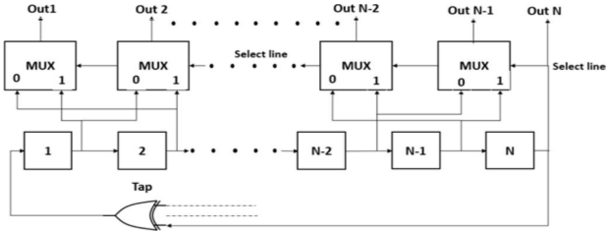


Figure 4: General architecture of BS-LFSR.

### 3.1.2 OUTPUT RESPONSE ANALYZER

An element of BIST called an Output Response Analyzer examines the outputs obtained from the CUT. The method most frequently used to examine CUT outputs is signature analysis.

**(i) Conventional MISR**

Signature analysis is carried out using the Multiple Input Signature Register (MISR). Divide the CUT output polynomial by the polynomial of the MISR to perform the MISR's function. The remainder is referred to as the golden signature or reference (manual calculation). The design of a conventional MlSR is shown in Fig. 3.3. Different output polynomials will exist for several output CUTs. Because of this, it will be challenging to analyse the

MISR's activity and confirm the golden signature. Additionally, if the number of outputs from the CUT exceeds the number of inputs, this conventional method will not work.

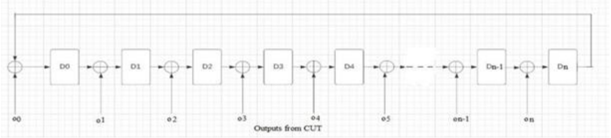


Figure 5: n-bit Conventional MISR.

**(ii) Modified MISR**

In this MISR, modification is accomplished by aggregating all of CUT's outputs into a single (result) polynomial, which is then fed into a Single Input Signature Register (SISR). All output polynomials are XORed at a point in the modified MISR, as shown in Fig.3.4 (aggregated). Because the resultant is a single polynomial, it is possible to trace the operation of MISR analytically. This MISRi overcomes the disadvantages of conventional MISR, particularly when the number of outputs of CUTs exceeds the number of inputs of MISR.

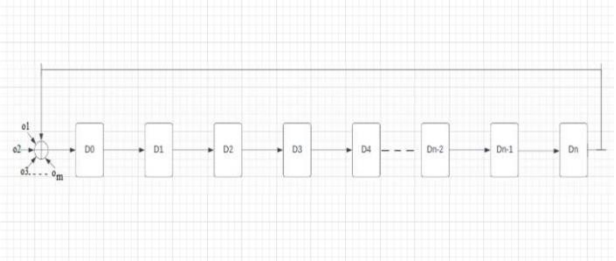


Figure 6: n-bit Modified MISR

### 3.2 DETERMINING THE POWEREFFICIENCY OF BS-LFSR

Here, we choose 4 bit conventional LFSR and BS-LFSR for determining the power reduction.

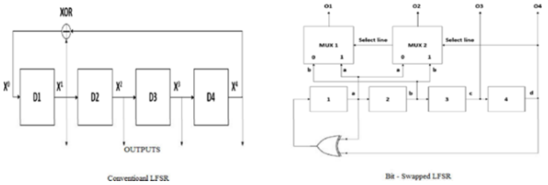
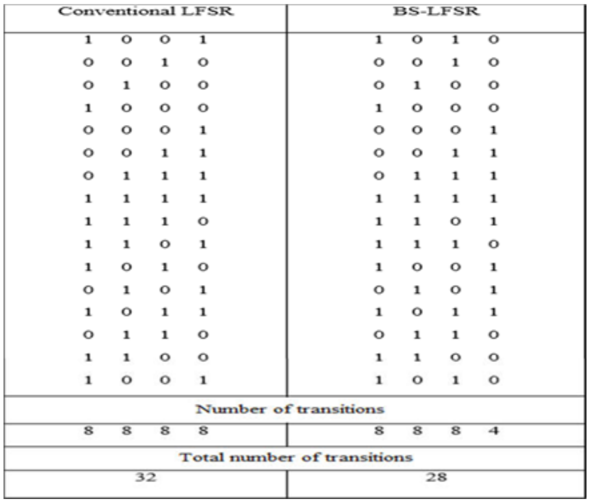


Figure 7: 4 bit conventional LFSR and BS-LFSR

#### 3.2.1 Comparison of LFSR and BS-LFSR Sequence

The conventional LFSR can produce a random sequence by choosing a proper feedback function.The period of sequence is 2n -1 for an n-bit LFSRi and the sequence is continuous and once the 2n -1 different values have occurred, it will repeat for the next sequence.

Similarly, In BS-LFSR, we add extra 2 x 1 multiplexers to the conventional LFSR so as reduce the switching activity or number of transitions. The basic idea is to move two neighbouring bits on a selected line value of the multiplexer. For this, We should consider one of its outputs as selected line(bit n) .If bit n = 1, there should not be any swapping. If bit n = 0,it should swap. Then when n is odd and bit n = 0, bit 1 will be swapped with bit 2, bit 3 with bit 4, and bit n-2 with bit n-1. If n is even and bit n = 0, bit 1 will be swapped with bit 2, bit 3 with bit 4, and bit n-3 with bit n-2.In all cases of the selection line bit n is excluded from the swapping operation. Below shown is the comparison table for initial seed 1001.



| Conventional LFSR | | | | BS-LFSR | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| Number of transitions | | | | | | | |
| 8 | 8 | 8 | 8 | 8 | 8 | 8 | 4 |
| Total number of transitions | | | | | | | |
| 32 | | | | 28 | | | |

Table 1: Comparison of LFSR and BS-LFSRi Sequence

The number of transitions in table 4.1 is reduced by four because of the switching activity.

As a result, based on equation(1), it will reduce the dynamic power dissipation in the BS- LFSR .

## IV. PROPOSED SYSTEM

### 4.1 Introduction

The design of a power-efficient BIST for an 8x8 BCD multiplier and combinational circuit is suggested in this work. Fig. 4.1 shows the fundamental design of the proposed BIST. In this BIST, the ORA is Modified MISR, and the TPG is BS-LFSR.

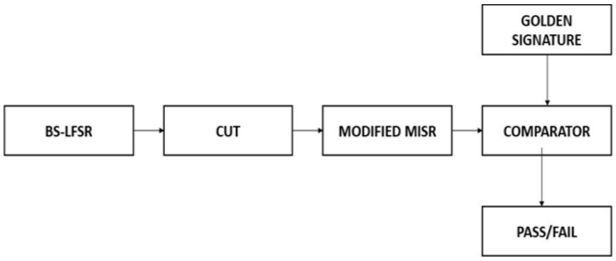


Figure 8: Architecture of proposed BIST

## 4.2 COMBINATIONAL CIRCUIT AS CUT

### 4.2.1 BS-LFSR as TPG

An n-bit maximal length LFSR will create a number of transitions equal to 2n−1 transitions at the output of each LFSRi cell if it begins with a non-zero seed and executes for 2n clock cycles to generate all conceivable test vectors. We alter the LFSR by treating one of its outputs (let's say bit n) as a selection line that, when the selection line has a given value (let's say 0), will swap two nearby bits elsewhere in the LFSR. Thus, bit 1 will be switched with bit 2, bit 3 with bit 4, bit n − 2 with bit n − 1 if n is odd and bit n = 0. Bit 1 will be switched with bit 2, bit 3 with bit 4,..., bit n − 3 with bit n − 2 if n is even and bit n = 0. The selection line—in this example, bit n—is never included in the switching process. No switching takes place if bit n = 1.

A regular LFSR and an additional 8x1 multiplexer are used to create the 16 bit BS-LFSR seen in fig. 4.2.

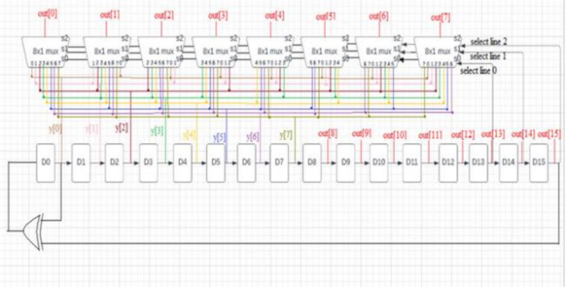


Figure 9: 16-Bit swapped LFSR

### 4.2.2. Circuit Under Test (CUT)

Fig. 4.3 is the CUT used for the BIST. This combinational circuit has eight outputs O[7:0].The patterns generated by the bit-swapped LFSR (initial seed= “1001010101010110”) are input to the CUT.

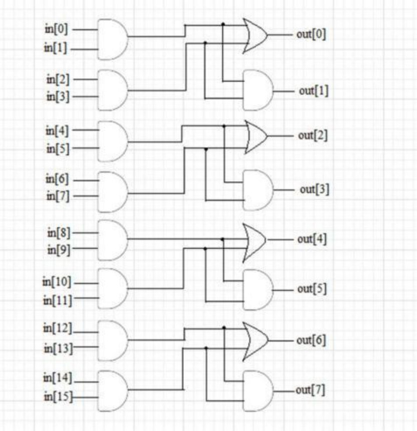


Figure 10: Circuit Under Test (CUT)

### 4.2.3. Modified MISR as ORA

The modified MISRi utilised for this BIST is seen in Fig. 4.4. Here, a SISR receives the result of aggregating (XORing) the CUT outputs, or O[7:0], at a certain point.By manually dividing the output polynomial of the CUT by the MISR polynomial, one may get the golden signature for this Modified MISR. The golden signature is provided by the remaining amount. The golden signature for the above CUT, when expressed in 16 bits, is 1110001101101011; the equivalent remainder is x15 + x14 + x13 + x9 + x8 + x6 + x5 + x3 + x + 1. Similarly, for a fault-free CUT, the golden signature may be determined by calculating the value of ORA in the 216th clock cycle following the production of the initial pattern [17].

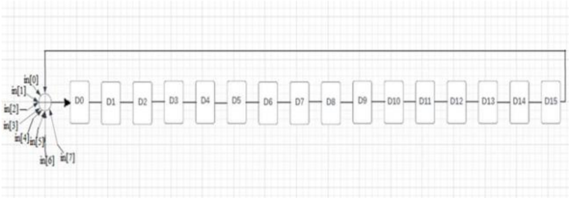


Figure 11: 16-Bit Modified MISR.

The proposed BIST is capable of detecting single stuck-at faults in a circuit. Because

this proposed method employs the stuck-at fault model, the circuit contains a single stuck-at fault. In this model, an input or output signal is set to ’0’ or ’1’.

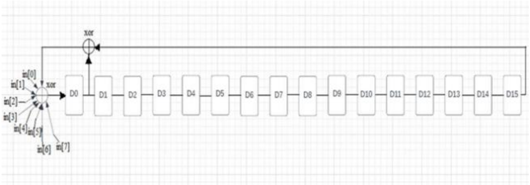


Figure 12: 16- bit Modified MISR

### 4.2.4 BS-LFSR as TPG

8- bit BS-LFSR shown in fig 4.6 is achieved by using a conventional LFSR and extra 4x1 multiplexers.

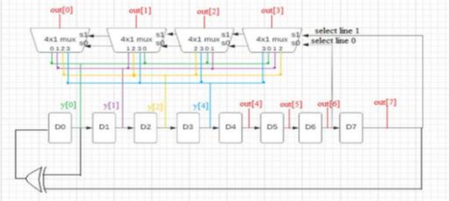


Figure 13: 8-Bit swapped LFSR

### 4.2.5 Modified MISR as ORA

The modified MISR employed for this BIST is displayed in Fig. 4. 7. Here, the outputs of an 8x8 BCD multiplier (CUT) are fed into a SISR after being aggregated (XORed) at a certain point.By manually dividing the output polynomial of the CUT by the MISR polynomial, one may get the golden signature for this Modified MISR. The golden signature is provided by the remaining amount. The equivalent remainder for the above CUT is x7 + x6 + 1, meaning that the golden signature is 11000001 when written in 8 bits. Similarly, for a fault-free CUT, the golden signature may be determined by calculating the value of ORA in the 28th clock cycle following the production of the initial pattern [17].

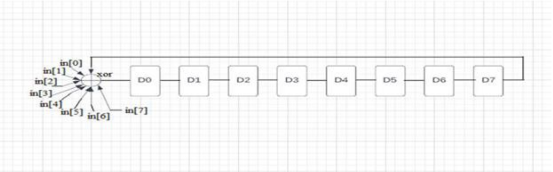


Figure 14 : 8-Bit Modified MISR

## V. RESULTS

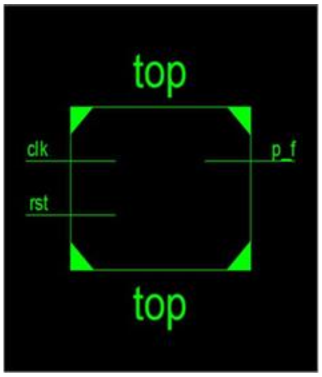


Figure 15. Top View

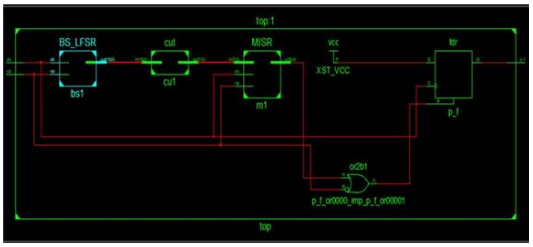


Figure 16. RTL Schematic

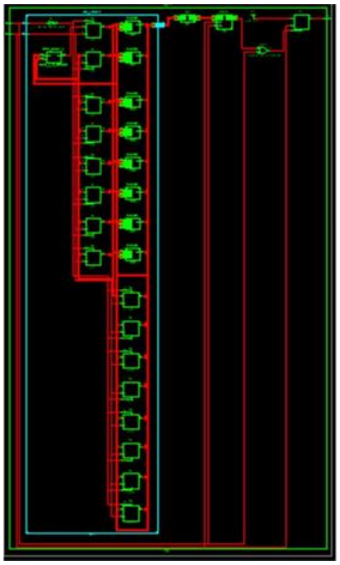


Figure 17. BS_LFSR Top View

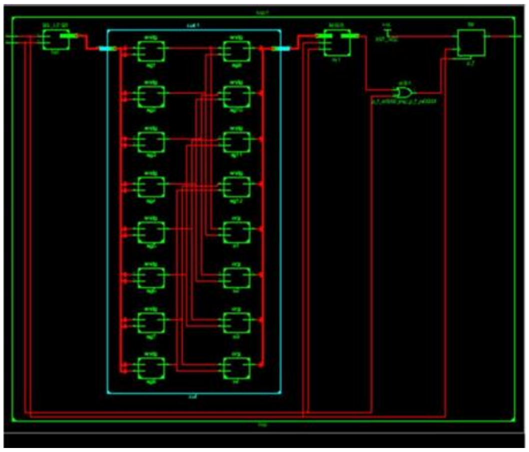


Figure 18. Top View of CUT

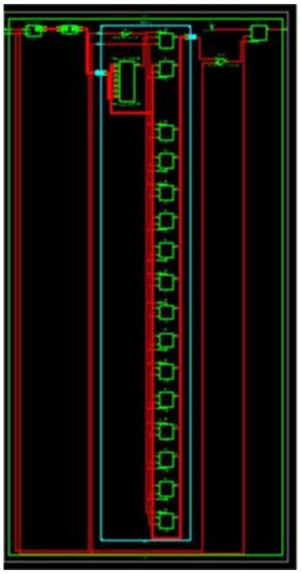
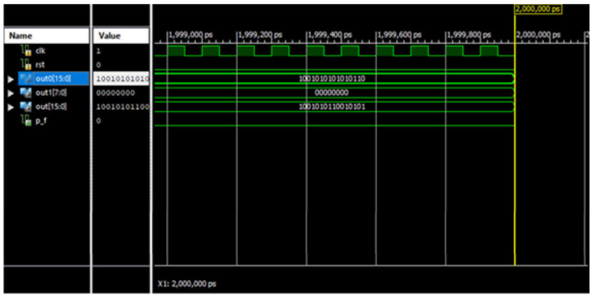
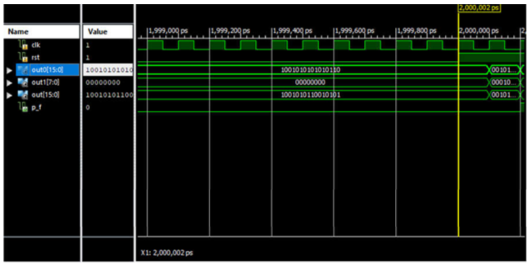


Figure 19. Top View of MISR



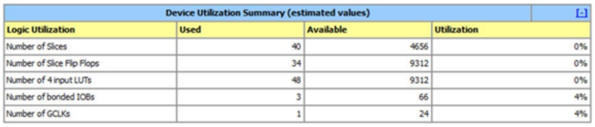
| Name | Value |
|---|---|
| clk | 1 |
| rst | 0 |
| out0[15:0] | 10010101010 |
| out1[7:0] | 00000000 |
| out[15:0] | 10010101100 |
| p_f | 0 |

Figure 20. BS_LFSR when Reset=0



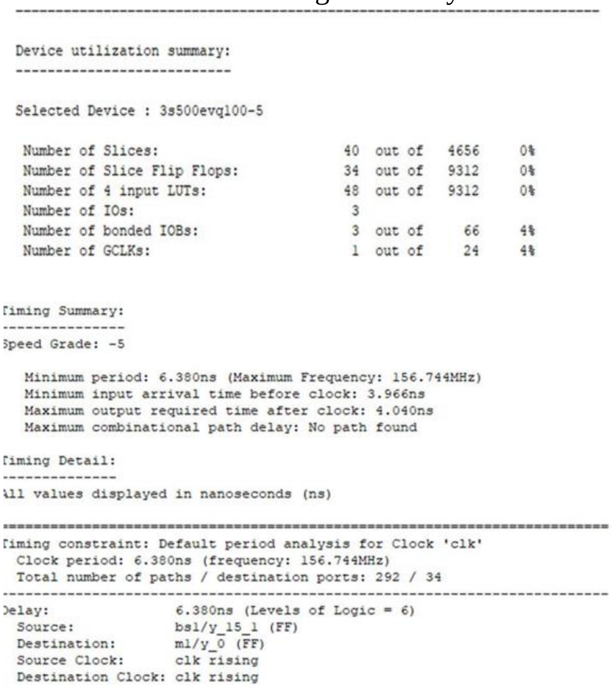
| Name | Value |
|---|---|
| clk | 1 |
| rst | 1 |
| out0[15:0] | 10010101010 |
| out1[7:0] | 00000000 |
| out[15:0] | 10010101100 |
| p_f | 0 |

Figure 21. BS_LFSR when Reset=1



| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 40 | 4656 | 0% |
| Number of Slice Flip Flops | 34 | 9312 | 0% |
| Number of 4 input LUTs | 48 | 9312 | 0% |
| Number of bonded IOBs | 3 | 66 | 4% |
| Number of GCLKs | 1 | 24 | 4% |

Table 2. Design summary



```
---------------------------------------------------------------------------

Device utilization summary:
---------------------------

Selected Device : 3s500evq100-5

 Number of Slices:                       40  out of   4656     0%
 Number of Slice Flip Flops:             34  out of   9312     0%
 Number of 4 input LUTs:                 48  out of   9312     0%
 Number of IOs:                           3
 Number of bonded IOBs:                   3  out of     66     4%
 Number of GCLKs:                         1  out of     24     4%


Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 6.380ns (Maximum Frequency: 156.744MHz)
   Minimum input arrival time before clock: 3.966ns
   Maximum output required time after clock: 4.040ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 6.380ns (frequency: 156.744MHz)
  Total number of paths / destination ports: 292 / 34
-------------------------------------------------------------------------
Delay:               6.380ns (Levels of Logic = 6)
  Source:            bsl/y_15_1 (FF)
  Destination:       ml/y_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising
```

Figure 22. Time summary

Figure shows the time summary of proposed method. Here, the proposed method consumed total 6.380ns of time delay, which is entirely route delay.

## VI. CONCLUSION AND FUTURE ENHANCEMENT

In this paper, we have explored the design and simulation of an area-efficient Built-In Self-Test (BIST) system that maximizes test coverage for modern integrated circuits. As semiconductor technology advances, ensuring the reliability of ICs becomes more critical, and the need for efficient, cost-effective testing solutions is paramount. BIST techniques have proven to be a valuable approach for automating testing and improving fault detection without the need for external test equipment. However, achieving the optimal balance between test coverage and area efficiency remains a significant challenge.

Through the integration of compression algorithms, test pattern generation strategies, and scan-based techniques, this paper has demonstrated that it is possible to create a BIST design that offers both comprehensive fault coverage and minimal area overhead. The proposed system leverages advanced simulation tools to evaluate and optimize the performance of the BIST architecture, allowing for the fine-tuning of design parameters to achieve better efficiency in fault detection while minimizing resource usage.

The results of this study highlight the importance of simulation-driven design in optimizing BIST systems. By employing simulation tools to explore different configurations, it is possible to identify the most efficient test patterns, reduce area consumption, and enhance fault detection across a wide range of failure modes. This approach ensures that even large, complex ICs, such as system-on-chips (SoCs) and microprocessors, can be tested effectively without imposing significant additional hardware or power requirements.

Despite these advancements, several challenges remain in further optimizing BIST designs. The trade-off between test coverage and hardware complexity continues to be an area of active research. Future efforts should focus on developing more advanced compression techniques, exploring machine learning and AI-driven optimizations, and investigating multi-layered BIST systems that can address the increasing complexity of modern ICs.

In conclusion, the proposed area-efficient BIST system represents a significant step forward in automated testing and fault detection for integrated circuits. By combining advanced simulation, compression, and optimized test patterns, this approach ensures that ICs are tested thoroughly, improving reliability and quality assurance without compromising on area efficiency or power consumption. This work lays the groundwork for the continued evolution of BIST techniques and offers a promising solution for the growing demands of modern semiconductor testing.

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