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# Energy-Efficient Dual-Edge Flip-Flop Design Using Single-Transistor Clocked Buffer in 22nm FD-SOI CMOS

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**ABSTRACT**

In the age of artificial intelligence (AI) and graphics processing units (GPUs), the flip-flop (FF) has emerged as one of the processor's most power-hungry elements. A innovative single phase-clock dual-edge-triggering (DET) FF employing a single-transistor clocked (STC) buffer (STCB) is suggested as a solution to this problem. The clock redundant transitions (RTs) and internal RTs present in previous DET designs are eliminated entirely by the STCB's use of a single-clocked transistor in the data sampling path. The suggested STC-DET beats the previous state-of-the-art low power DET in power consumption by 14% and 9.5%, at 0.4 and 0.8 V, respectively, when running at 10% switching activity, as shown by post-layout simulations in 22 nm fully depleted silicon on insulator (FD-SOI) CMOS. Among the DETs, it also attains the lowest power-delay-product (PDP).

**Keywords:** Flip-Flop (FF) Optimization, Dual-Edge Triggering (DET), Low-Power Design, Single-Transistor Clocked Buffer (STCB), Clock Redundant Transition Reduction.

## 1. INTRODUCTION

The low-power redundant-transition-free TSPC dual-edge-triggering flip-flop using single-transistor-clocked buffer was proposed by Zisong Wang, Peiyi Zhao, and the rest of their research team at the Fowler School of Engineering, Chapman University, Orange, CA 92866, USA.

In coming days, Power consumption is major concern in digital electronics. Based on digital electronics microprocessors and micro-controller chips are major role. If we can reduce power consumption in these chips then overall device power consumption is decreases.

In modern high-performance processors, flip-flops are one of the major sources of power consumption. This is because FFs are constantly switching to capture data at the rising and falling edges of the clock signal. To reduce the power consumption of FFs, a number of low-power FF designs have been proposed.The Low-Power Redundant-Transition-Free TSPC Dual-Edge-Triggering Flip-Flop, employing a Single-Transistor-Clocked Buffer, represents a sophisticated circuit design aimed at minimizing power consumption and enhancing reliability in digital systems. This innovative flip-flop leverages dual-edge triggering for efficient signal processing while strategically integrating a single-transistor clocked buffer to optimize power efficiency. The redundancy elimination ensures a smooth transition between states, contributing to the overall reliability of the flip-flop. This introduction sets the stage for a comprehensive exploration of the features and advantages inherent in this cutting-edge circuit design, especially when facing the drive from modern graphics processing unit

(GPU)/artificial intelligence (AI) neural network processors. The computing power used in AI training has doubled every 3.4 months.

Conventional single-phase-clock FFs only use one clock edge in a time period to process input data, resulting in an unnecessary power overhead as the other clock edge stays undeveloped for data processing. Dual Edge-Triggering (DET) FFs take advantage of both clock edges to process data, thus can lower clock frequency to half for reducing power consumption while still maintaining the same throughput.

In DET FFs, one of the power consumption issues is that the clocked transistors often cause unnecessary redundant power consumption overhead which occurs when input data remain unchanged but some transistors in the circuit still switch actively due to the circuit topology,to reduce the aforementioned redundant clock transition power in dual-phase-clock DET, a few single-phase-clock DET FFs have been proposed to avoid the cascaded clocked inverters. One of the approaches is the FS TSPC DET.There is no explicit clocked inverter in FS TSPC, as only one clock phase is used. However, when input does not change, there is an implicit internal RT.If D stays at 1, D P will stay at 0, then the NOR structure in the middle of figure becomes an inverter that has one clocked PMOS and one clocked NMOS. The implicit-redundant transition has thus occurred because of the continual switching of the two clocked transistors. Similarly, if DN stays at 1, the NAND structure will become an inverter which will also have the constant switching problem, causing the implicit-redundant transition. Another static true-single-phaseclock DET, TSPC DET, also suffers from the implicit-redundant transition in a similar mechanism.

We use Redundant Transition in Two-Phase-Clock DET, where two cascaded inverters are used to generate the two clock phases. However, when input data do not change, the cascaded inverters remain switching constantly, resulting in clock RT power [13]. As an example, this redundant-transition behavior existing in FN_C-DET. Furthermore, there is a contention, which is a type of short circuit, between outer-C-elements (N1, N4, P1, P4) and inner-C-elements (N2, N3, N4, P2, P3, P4) at node B during transition time in FN_C-DET.

## 2. LITERATURE REVIEW

AI and compute byAI and Compute from 2018 by OpenAI discuss the relationship between the progress in AI capabilities and the computational power (compute) used to train AI models. OpenAI highlights the trend that over the years, the amount of compute used in large AI training runs has been increasing exponentially, often referred to as "Moore's Law for AI." The post discusses the implications of this trend, including the environmental impact, the cost of AI research, and the potential concentration of AI capabilities in organizations with access to large computational resources. It's an interesting read if you're into the intersection of AI development, technology, and its broader implications.

An energy-efficient high-performance ×86 core by T. Singh et alAMD's next-generation, high-performance, energy-efficient ×86 core, Zen, targets server, desktop, and mobile client applications with a 52% instructions per clock cycle (IPC) uplift over the previous generation. The increase in IPC complements a 15% process neutral reduction in CAC (switching capacitance). Performance and energy efficiency are further improved with various circuit techniques including write word line boost, contention-free dynamic logic, supply droop detection with mitigation, a per-core frequency synthesizer, and a per-core integrated linear voltage regulator. Utilizing a 14 nm FinFET process, the Zen core complex unit consists of a shared 8 MB L3 cache and four cores.

New low glitch and low power DET flip-flops using multiple C-elements byS. Lapshev and S. M. R. Hasan The designs of static dual-edge-triggered (DET) flip-flops that exhibit unique circuit behavior owing to the use of C-elements. Five novel DET flip-flops are presented including two high-performance designs and designs that improve upon common Latch-MUX DET flip-flops so that

none of their internal circuit nodes follow changes in the input signal. A common characteristic of the presented flip-flops is their low energy dissipation due to glitches at the input. Novel DET flip-flops are compared to existing DET flip-flops using simulation in a high performance 28 nm CMOS technology and are shown to have superior characteristics such as power and power-delay product (PDP) for a range of switching activities. Extensive Monte Carlo and voltage scaling simulations are performed to show that the presented designs are robust under PVT variations.

Comparative delay and energy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microprocessors by J.Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev. A low conditional discharge(C-element) Flip-Flops that are basic elements in all digital design. The existing circuits are power hunger due to the dynamic and static power dissipation increases. For reducing power consumption C element technique is used to reduce glitches at the data out. Results obtained through 130nm technology shows reduction in energy dissipation and delay. Average dynamic power dissipation of the proposed flip-flop is compared with two existing techniques. Average power of proposed flip-flop is reduced by 28.41% and 36.18% when compared with Latch-Mux flip-flop and Latch-Mux using C-element.

High-performance and low-power conditional discharge flip-flop by P. Zhao, T. K. Darwish, and M. A. Bayoumi. High-performance flip-flops are analyzed and classified into two categories: the conditional precharge and the conditional capture technologies. This classification is based on how to prevent or reduce the redundant internal switching activities. A new flip-flop is introduced: the conditional discharge flip-flop (CDFF). It is based on a new technology, known as the conditional discharge technology. This CDFF not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining the negative setup time and small D-to-Q delay characteristics. With a data-switching activity of 37.5%, the proposed flip-flop can save up to 39% of the energy with the same speed as that for the fastest pulsed flip-flops.

A fully static topologically-compressed 21-transistor flip-flop with 75% power saving by N. Kawai et al. An extremely low-power flip-flop named topologically-compressed flip-flop (TCFF) is proposed. As compared with conventional flip-flops, the novel FF reduces power dissipation by 75% at 0% data activity. This power reduction ratio is the highest among FFs that have been reported so far. The reduction is achieved by applying topological compression method, merger of logically equivalent transistors to an unconventional latch structure. The very small number of transistors, only three, connected to clock signal reduces the power drastically, and the smaller total transistor count assures the same cell size as conventional FFs. In addition, fully static full-swing operation makes the cell tolerant of supply voltage and input slew variation. An experimental chip design with 40-nm CMOS shows that almost all conventional FFs are replaceable with proposed FF while preserving the same system performance and layout size.

Ultra-low power 18-transistor fully static contention-free single-phase clocked flip-flop in 65-nm CMOS Author: y. Cai, A. Savanth, P. Prabhat, J. Myers, A. S. Weddell, and T. J. Kazmiersk. Flip-flops (FFs) are essential building blocks of sequential digital circuits but typically occupy a substantial proportion of chip area and consume significant amounts of power. This paper proposes 18-transistor single-phase clocked (18TSPC), a new topology of fully static contention-free single-phase clocked (SPC) FF with only 18 transistors, the lowest number reported for this type. Implemented in 65-nm CMOS, it achieves 20% cell area reduction compared to the conventional transmission gate FF (TGFF). Simulation results show the proposed 18TSPC is two times more efficient than TGFF in the energy-delay space. To demonstrate EDA compatibility and circuit/system-level benefits, a shift register and an AES-128 encryption engine have been implemented. Chip experimental measurements at 0.6 V, 25 °C show that, compared to TGFF, the proposed 18TSPC achieves reductions of 68% and 73% in overall and clock dynamic power, respectively, and 27% lower leakage.

A 65-nm pulsed latch with a single clocked transistor by M. Saint-Laurent, B. Mohammad, and P. Bassett. The logy limits placed on the clock switching energy in sequential elements. It proposes a novel pulsed latch that uses a single clocked transistor and consumes close to ten times less clock power than a conventional latch using six clocked transistors. It describes how the new circuit enables additional power savings when virtual grounds, instead of a regular clock, are locally distributed to a group of latches. Finally, the paper discusses how to further reduce the dynamic clock power consumption of the new latch without degrading its timing by feeding it a low-swing clock.

Title: A novel design for ultra-low power pulse-triggered D-flip-flop with optimized leakage power by A. Karimi, A. Rezai, and M. M. Hajhashemkhani, the power efficiency and reducing the layout area are two main concerns in D-Flip-Flops (D-FF) design. In this paper, a novel architecture is presented for the pulse-triggered D-FF in the CMOS 90-nm technology. This novel architecture utilizes a transmission gate to control the input data and the leakage power. The Pulse Generator (PG) is also modified to reduce the number of required transistors and the clock pulse delay. In addition, the pull-up P-MOS transistor is controlled by input data to reduce the power dissipation. The proposed D-FF is simulated using Hspice. The simulation results show that the proposed architecture has improvement in terms of power consumption, D-to-Q delay, and Power Delay Performance (PDP) in comparison with other D-Flip-Flop architectures.

Ultra-low power pulse-triggered CNTFET-based flip-flop by A. Karimi, A. Rezai, and M. M.Hajhashemkhani. Reducing the power consumption and scaling the devices are the important concerns of today's electronics. Flip-Flop (FF) is one of the basic elements in electronic devices. Thus, the performance of the electronic devices is improved by improving these qualities in the FFs. In this paper, a novel pulse-triggered CNTFET-based D-Flip-Flop structure is proposed. This structure utilizes signal feed through technique to reduce the “0” to “1” transition, which requires only one CNTFET. Moreover, the discharging path is optimized to reduce the delay time for “1” to “0” transition by using only two CNTFETs. The novel structure is simulated in Hspice using Stanford model. The output results prove that the performance of the proposed structure is improved greatly in terms of power consumption, D-to-Q delay, the power-delay product, and the number of required transistors in comparison with other pulse-triggered Flip-Flop structures.

Low-power clocked-pseudo-NMOS flip-flop for level conversion in dual supply systems by P. Zhao et al Clustered voltage scaling (CVS) is an effective way to decrease power dissipation. One of the design challenges is the design of an efficient level converter with fewer power and delay overheads. In this paper, level-shifting flip-flop topologies are investigated. Different level-shifting schemes are analyzed and classified into groups: differential style, n-type metal-oxide-semiconductor (NMOS) pass-transistor style, and precharged style. An efficient level-shifting scheme, the clocked-pseudo-NMOS (CPN) level conversion scheme, is presented. One novel level conversion flip-flop (CPN-LCFF) is proposed, which combines the conditional discharge technique and pseudo-NMOS technique. In view of power and delay, the new CPN-LCFF outperforms previous LCFF by over 8% and 15.6%, respectively.

A fully static true-single-phase-clocked dual-edge-triggered flip-flop for near-threshold voltage operation in IoT applications by Y. Lee, G. Shin, and Y. Lee A Dual-Edge-Triggered (DET) flip-flop (FF) that can reliably operate at low voltage is proposed in this paper. Unlike the conventional Single-Edge-Triggered (SET) flip-flops, DET-FFs can improve energy efficiency by latching input data at both clock edges. When combined with aggressive voltage scaling, significant efficiency improvement is expected. However, prior DET-FF designs were susceptible to Process, Voltage and Temperature (PVT) variations, limiting their operation at low voltage regimes. A fully static true-single-phase-clocked DET-FF is proposed to achieve reliable operation at voltages as low as a near-threshold regime. Instead of the two-phase or pulsed clocking scheme in conventional DET-FFs, a True-Single-Phase-Clocking (TSPC) scheme is adopted to overcome clock overlap issues.

## 3.PROPOSED MODEL

The flip-flop is become the power consuming block in the Graphical Processer, Artificialintelligence (AI) era and other Electronic Devices. In this project we are going to reduce the power consumption of flip-flop. In this process we reduce the number of transistors used inflip-flops. By reducing the number of flip-flops, the switching activity will decrease, then the power consumption will also decrease. The low power consumption of the circuit will lead to better performance of the device.To eliminate the aforementioned redundant transitions between two clocked transistors (one PMOS, one NMOS) in dual-edge FFs, a lowpower TSPC DET FF is proposed with innovative redundant-free STCB topology.

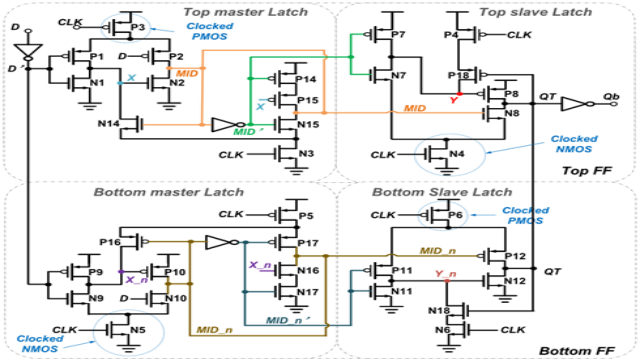


Fig. 4. Proposed TSPC single transistor clocked DET, STC-DET.

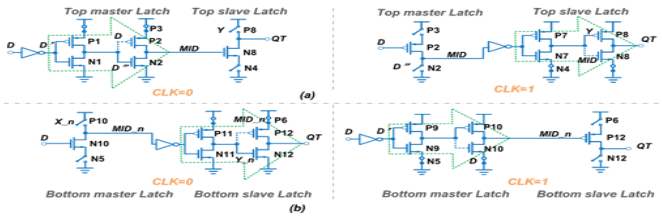


**Figure 1. Operation of the proposed STC-DET: (a) Top FF and (b) bottom FF using equivalent simplified logic circuit diagram**.

### 3.1 Operation of the Top FF in STC-DET

When CLK = 0, in the data sampling path of the top FF, the clocked PMOS P3 in the top master latch turns on, node X becomes D″ (see the top left of Figure 1); since D″ is essentially D, then transistors (P2, N2) will become equivalent to a virtual inverter [A simplified logic diagram is illustrated in Fig. 1]. Then the input passes to MI D in the top master latch (see arrow in the top left of the above figure); On the other hand, in the top slave latch in Fig. 1, clocked NMOS N4 is off since CLK = 0, so node Y will not be 0, hence PMOS P8 is off. QT is not connecting with VDD or GND, meaning that QT in the top FF is floating (see the top left of Fig. 1).In Fig. 1, transistors (N1, N2, P1, P2, P3) build a negative triggered STCB, where only one clocked transistor P3 is used in signal sampling path. The RT which occurs between one clocked PMOS and one NMOS in FN_C DET and FS-TSPC, Fig. 1, does not exist in STCDET. Neither is there any contention. Besides the clocked transistor P3, there is one more clocked NMOS transistor N3, in the top master latch (see the top left of Fig. 1), but it is used in keeper, rather than the data sampling path. All the four clocked transistors that are on the data sampling path have been marked out with an arrow in Fig. 1 (P3, N4, N5, and P6).Transistors (N4, N7, N8, P7, P8) build another positive triggered STCB in the top FF.When CLK = 1, in the top master latch in Fig. 4, clocked PMOS P3 is off since CLK = 1, so the paths associated with P1 and subsequently N2, are off. As a result, the logic state of MI D is kept by keeper (N3, N15, P14, P15). When X's logic state is 0, it will be kept by pull down keeper (N14, N3). On the other hand, in the top slave latch, the clocked NMOS, N4, turns on, so Y is MI D″ which is essentially MI D. Therefore, transistors (N8, P8) act as a virtual inverter, the signal of MI D which is right before clock rising edge passes to QT (see the arrow in the top right of the Fig. 1). Hence, the top FF is activated at the clock positive edge.

### 3.2 Operation of the Bottom FF in STC-DET

When CLK = 0, in the bottom FF (see bottom left of Fig. 1), the clocked NMOS, N5, in the bottom master latch turns off. Consequently, the paths associated with N9 and P10 are off, and the logic state of MI D_nis kept by keeper (N16, N17, P5, P17); if logic state of X_nis 1, that state will be kept by pull up keeper (P16, P5). On the other hand, in the bottom slave latch (bottom right of Fig. 4), clocked PMOS P6 in top of the figure turns on when CLK = 0, Y_nbecomes MI D_n″ which is essentially MI D_n, thus P12 and N12 act as a virtual inverter, and the signal of MI D_nwhich is right before clock falling edge passes to QT (see arrow in the left half of Fig. 1). As a result, the bottom FF is activated on clock negative edge. There would be no redundant transition if D keeps the same value since it causes no switching.Transistors (N5, N9, N10, P9, P10) and (P6, N11, N12, P11, P12) build other two STCBs in the bottom FF.When CLK = 1, the clocked NMOS N5 in the bottom master latch turns on (see the bottom left of Fig. 4), X_nwill be D″ which is essentially D, thus P10 and N10 act as a virtual inverter, and input D passes to MI D_nin the bottom master latch [see arrow in right half of Fig. 1]; On the other hand, the clocked PMOS P6 in the bottom slave latch turns off, so the paths associated with P11 and subsequently N12 will also be off. And it is worth mentioning that as QT node has another connection in the top FF which is active when CLK = 1 as discussed before, QT is a nonfloating node. There is still no redundant transition if D keeps the same value since it does not affect QT.Since the top and bottom slave latches are activated by positive clock edge and negative clock edge, respectively, STC-DET can sample input at both edges of clock. Moreover, because the two slave latches are activated by different clock edges, so there is always one latch that is transparent and the other one is opaque for all periods, thus the slave latches' outputs can be connected together at QT without contention. Furthermore, this transparent connection to supply or ground for QT makes it an all-time nonfloating node. And if necessary, by adding an enable signal and scan input to the master latches on the left side, one can easily modify STC-DET to be scannable for supporting the design for test (DFT). Also, by adding keepers at the end of the top or bottom FF, it can be modified into a single-edge FF design, respectively.

## 4. RESULTS& DISCUSSION

Simulation results provide a comprehensive understanding of how the designed circuit behaves under different conditions. They are crucial for verifying the functionality, identifying and resolving issues, and ensuring that the circuit meets the desired specifications before physical implementation. Figure 2 shows the simulation results of the proposed system.

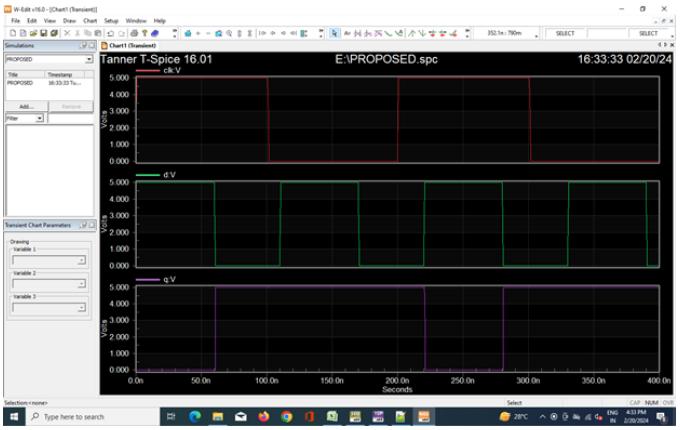


**Figure 2: Simulation results of the proposed system**

The block diagram offers a high-level representation of the entire system, illustrating the functional blocks and their interconnections. It serves as a visual guide for system architecture, aiding designers in

conceptualizing and communicating the design structure and functionality. Figure 3 shows the block diagram of the proposed system.

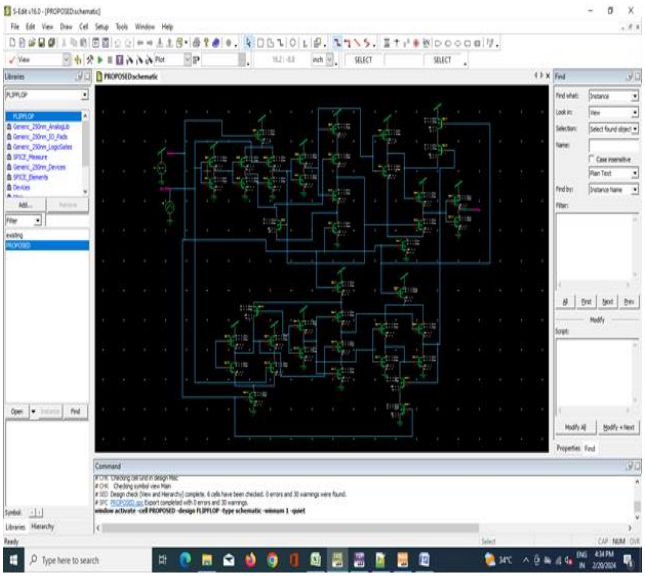

**Figure 3: Block diagram of the proposed system**

Power consumption is a critical consideration in modern VLSI design. Estimating power consumption helps designers optimize the design for power efficiency, which is crucial for battery-operated devices and minimizing environmental impact. Power estimation also guides decisions on cooling mechanisms.The power consumed in the circuit is 0.058w.

Delay estimation is essential for ensuring that the designed circuit meets timing requirements. It helps identify and address timing issues such as setup and hold time violations, ensuring that signals propagate through the circuit within the specified time constraints.The delay in the circuit is 1.179ns. The power and delay estimation results are shown in figure 4.

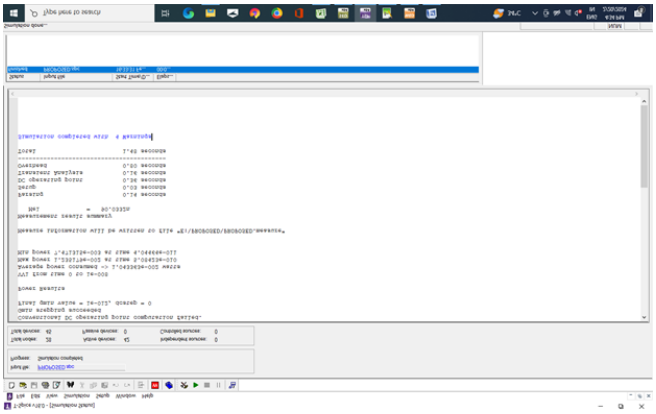

**Figure 4: Power and Delay estimation of the proposed system**

## 5. CONCLUSIONS

To completely eliminate RT in dual-edge-triggered FFs, a novel low-power redundant-transition-free dual-edge-triggered FF is proposed, namely STC-DET, as it uses STC buffers. Of the twoSTC buffers inside the topology (the positive-triggered one and the negative-triggered one), each has only one clocked transistor in the data sampling path, leading to a complete removal of clock redundant transitions and internal redundant transitions that existed between two clocked transistors in other DET designs. Furthermore, there is no contention in the proposed STC-DET. In view of power consumption, STC-DET dissipates less power than the prior state-of-the-art FN_CDET by 14% and 9.5% at switching

activity of 10% in 0.4, 0.8 V, respectively. Also, STC-DET consumes the least amount of power in all process corners, different voltages (0.4–0.8 V) for switching activities below 20% among all DET designs. Regarding PDP (C Q), the proposed design outperforms FN_C-DET by 53.4%, 51.0% at 10% switching activity with 0.4 and 0.8 V, respectively. In summary, the proposed STC-DET achieves the lowest power consumption and PDP in the average switching activity range among all the DET FFs of the state-of-the-art.

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